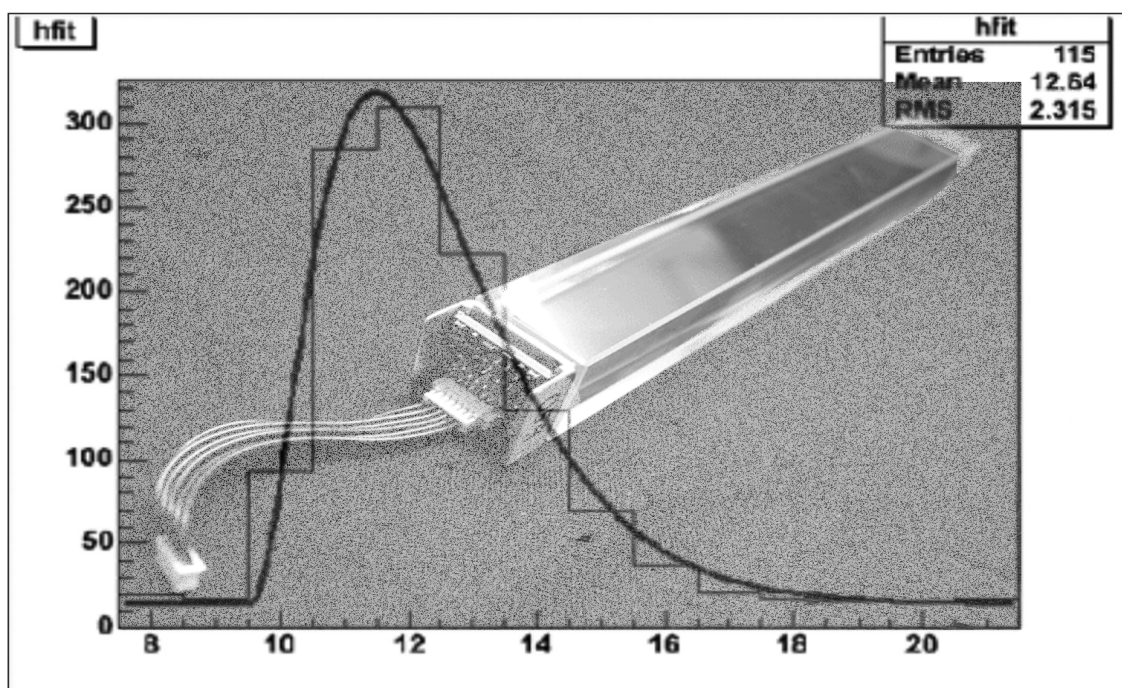


PHOS

PHOS basics for the user

Revision 4

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1 PHOS parameters overview.

Table 1 PHOS FEE, geometrical and mechanical data

PHOS component	Dimensions /Data	Details
1 PHOS module	$\Delta z \Delta \phi = 56 * 64$ PWO crystals $\Delta \eta \Delta \phi = 0.24 * 20^\circ$ Fiducial crystal surface $0,722 * 1,263 \text{ m}^2$	3584 crystals/ module
P_bWO₄ crystal Chapter 1.8	$22 * 22 * 180 \text{ mm}^3$ inorganic scintillator crystals 440 nm (blue) and 530 nm (green) light decay time 10.6 ns @ room temperature. Radiation length $X_0 = 0.89 \text{ cm}$. Max. incident photon angle per crystal <13 degrees	radiation lenght for 20 cm ~ 18 100um stainless steel /Tyvek wrapping Moliere Radius 2.0 cm crystal weight: 721.3 g Light yield for 2004 production (Apatity) ~ 12 pe/MeV heat conductivity 1.43 W/mK. heat capacity is 271 J/kgK
double strip unit footprint	$45.1 * 180.4 \text{ mm}^2$	2 * 8 crystals, double T-cards
T-cards and connectivity Chapter 13	<u>Old</u> : $170 * 50 \text{ mm}^2$ 8 CSP connectors / T-card 1 AMP base connector <u>New</u> : double T-card 16 crystalsCSP cables / 1 x 60 pin base connector <u>Jumper cables</u> : a.) Molex connectors 1.25 mm PicoBlade Friction Locking Receptacle housing No 51021-0600, 6 contacts b.) contacts: female Crimp terminal 50079-8000 on a reel for 26-28 AWG wire c.) cable: 6 cm Paige Electric LL43774 , AWG 24, 300 Volt) Connection type: pin1-pin1, pin2-pin2, etc <u>CSP connector on T-card</u> : Molex Picoblade 1.25 mm header 6-pin 53047-0610	<u>Old</u> : Base connector: 37 pin 2.76 mm AMP / Tyco Board Mount Connector (747 470-2) <u>New</u> : Wiremount T-card connector 60 pin 3M 3334-6600 <u>flat cable</u> : 0.45 m 3M reference 2010-60 halogen-free 60 wire <u>Wiremount FEE adapter- connector</u> 60 pin: 3M reference 3334-6000 <u>Boardmount T-card connector 60 pin</u> : 3M 60 pin 3M reference: N2560-6002RB <u>Boardmount connector FEE adapter side</u> : 3M reference N3372-6202RB
Feedthrough flat cable T-card<>FEE	<u>Old</u> : ca. 20 cm long 2 Flat cables 40 wire CERN SCEM 04.21.22.340.3 reduced to 37 pin 1.27mm pitch <u>New</u> : 60 wire 3M cable 20010/60, halogene-free, ca 45 cm long, direct connection to double T-card and to FEE adapter board. FEE adapter connector: 3M type: N3372-6202R	<u>Old</u> : Cable T-card side: 37 pin fem. 3M 8337-6009 CERN SCEM 09.21.20.130.9 FEE side: solder to intermediate PCB adapter <u>New</u> : IDC cable with 2x30 pin connector & 16 inch lenght: Samtec generic type would be IDSD-30-D-18.00 but 2x30 is not standard: use 3M cable 20010/60
Warm Volume	$1310 * 1490 * 245 \text{ mm}^3$	Encloses 112 FEE and 8 TRUcards, 8 GTL bus strips (the RCU and Trigger OR is outside)
New FEE adapter card (IPCB replacement)	<u>Old</u> : Left and Right adapter PCB for flat cable to FEE connector: max $90 * 630 \text{ mm}$ PCB strips with mounting holes <u>New</u> : two adapters per FEE card top and bottom	<u>Old</u> : FEE mating connector on IPCB: Samtec LS2-130-01-S-D 14 connectors @45.4 mm pitch <u>New</u> : 2 x 30 pin 2 mm solder-connector between FEE and adapter card: Samtec TMM-130-01-T-D, cable connector 3M type: N3372-6202R.
FEE card Chapt 9	<u>Old</u> : 32 channel front-end electronics cards HUST / CERN, 1 us shaper CERN No. 0000042476 V1.1a $349 * 210 \text{ mm}^2$ <u>New</u> : FEE V1.1b $353 * 210 \text{ mm}^2$ PhOS 1 us shaper, adapter card to front end <u>New</u> : V1.1e $353 * 210 \text{ mm}^2$ EMCal 100 ns shaper, LS2 connector to backplane	10 Layer PCB, FR4 (or S1155 Halogene free) , Weight 450 gram with copper cassette: 1.2 kG Input: two 60 -pin connectors Samtec LS2-1-30-01-S-D-RA1 <u>New</u> : LS2 connector replaced by adapter card with 3M type cable connector N3372-6202R

Table 1 PHOS FEE, geometrical and mechanical data

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GTL bus strips Chapt 10	50 line GTL+ Data bus, termintated 75 OHM 54*630 mm 26 line GTL+ Control bus, terminated 75 OHM 30(43)*630 mm	Cadence Allegro .brd file reference: eda0711_Long_cx20050513 data bus 50 lines eda0712_Long_cx20050513 Control bus 26 lines (short test version also available)
TRU	Trigger Region Unit (TRU) 353 * 210* 2 mm ² , 30 Watt RJ45 LVDS output: Level-0 and 3 x Level-1 112 differential inputs from FEE Fast OR(analog sums) converted by 40 MHz ADCs to 112 x 12 bit serial linesto single Virtex FPGA.	14 layers PCB, FR4 or halogene-free weight with power radiators ca. 1 kg 14 octal analog sum cables of equal length connect 1 TRU with 14 FEE cards Fast Or cables: Samtec FFSD-08-D-20m, 16 pin, 1.27 mm, 40 cm
TRU domain	16*28 crystals = 14 FEE cards 59*36 cm	1 of 8 local trigger domains of a PHOS module
CSP Preamplifier Chapter 3	19 * 19 mm ² attached to PWO crystal via soldered APD on back side, glued to crystal. 6 pin cable connector	Discrete logic on printed circuit contamination-free Matsushita R-4726 bromine or chlorine 6 way Molex connector 53047-0610
APD Chapters 1.3	Hamamatsu S8664-55 (S8148) 5 * 5 mm ² ceramic, 10.6 mm	glued to PWO with Quick Stick, n= 1.7b

Table 2 Electrical parameters PHOS FEE electronics

Component	Properties	details
CSP preamplifier (-25 C) Chapter 1.4	0.833 V/pC or 0.133 uV / e- 64 mW +12 V - 4.2 mA -6 V - 2.2 mA ENC = 200 e + 3.2 e / pF * C _{in} (pF) -> 520 electrons at C _{in} =100 pF linearity range 0.1 mV- 5.0 V U _{csp} [uV]=M*0.533 / MeV +69	C _i = 1.2 pF (effective) Input JFET : 2SK932 C _{in, FET} = 10 pF (FET) C _{Det} = 100 pF (CSP+APD) M= APD gain nominal value M=50 3584 CSP's generate 215 Watt heat in the cold volume
APD diodes (-25 C) Chapter 1.3	APD light yield: for nominal crystal L.Y =10 ~4 pe-/MeV @ gain = 1 200 pe -/ MeV @ M=50 (Excess Noise factor F = 2.27)	S8664-55 Hammamatsu (S8148) M=50 for 330-395 V @ -25 °C C _{APD} = 90 pF Breakdown Voltage > 400 V
RMS noise and Pedestals after shaper at -25 C Chapter 4	Pedestal average high gain: 35+-10 ADC counts. low gain: 55 +-10 ADC counts Best measured single channel (purified) RMS noise taken from pre-samples with APD @ -25 C and 2 us peaking time: 340 electrons (1.5 MeV) -> 3x3 noise 4.5 MeV. Average 3x3 noise less 10 MeV. The offline 3x3 noise from 2006 testbeam at -16 C taken from pedestal runs meas- ured indirectly ~10 MeV	APD operated at 350 Volt and C _{DET} = 100 pF, T = -25 C: I _{dark} <1 nA, M=50 8 pre-samples used for RMS determina- tion, crosstalk and pileup events were dis- carded.
Dynamic range Chapter 1.4	single channel design value: 5 MeV.....81.92 GeV (= 2 ¹⁴) -> 14 bit true single channel range with measured gain ratio 16.83: 5MeV to 86.16 GeV high gain: 5MeV - 5.12 GeV low gain: 84.15 MeV - 86.17 GeV full range (including showe leakage esti- mated 5 MeV - 100 GeV.	design ratio High/Low-gain = 16/1, measured: 16.83 digital resolution (bitvalue/1024) < σ/E
CSP linear voltage ranges	for fixed shaper gain x APD-gain M=50: 5 MeV - 5.12 GeV : 0.137 mV - 0.1407 V (shaper gain=7.2) 80 MeV - 81.92 GeV: 2.19 mV - 2.245 V (shaper gain =0.45)	Gain for high energy range is set to 80 GeV max. single channel (= 100 GeV for a central γ) Gain ratio = 16 -> LSB set to 5 MeV
Zero-pole cancellation Chapter 3	pole-zero time constant at shaper meas- ured = 67 us. Undershoot low Energy < 0.8% Overshoot high Energy 0.5 - 2.5 %	pole-zero cancels shaper signal under- shoot due to autotidcharge time constant of CSP and due to ground-level offsets (linearity)
Shaper 1 us Chapter 5	Filter Order: n=2, 1 us shaping time bandwidth (-6 dB) 500 kHz τ _{peak} = 2.143+-0.015 us Bandpass f _c = 159 kHz high gain = 7.2 (low Energy) low gain = 0.45 (high Energy) Dynamic range 14 bit pedestal low Energy : 26.5 ADC pedestal high Energy: 35+-10 ADC Linearity <<0.5 % differential timing resolution: <= 2 ns @ 400 ADC counts (~ 2 GeV) (preliminary)	second order Bessel low-pass with pre- ceding RC high pass, -20 db < f _c < -40 db pole-zero compensation, fully differential output to Altro ADC with 1 Volt window/10 bit
channel rate @ E_{cut}>50 MeV p-p Chapter 10.1	20 Hz	see Figure 83 for Pb-Pb @ 5 TeV
digitizer Chapter 9	Altro-16, ST Microelectronics 16 * 10 bit, ENOB = 9.7 bit for input BW < 1MHz.	Based on 10 bit, 25 MHz ST Microelec- tronics ADC cell TSA 1001. 15 mWatt/ADC noise < 0.4 ADC cnt. measured on FEE card without detector

Table 2 Electrical parameters PHOS FEE electronics

Component	Properties	details
Energy calibration	LSB = 5 MeV 5 MeV / bit for CW shaper with nominal APD gain M=50	1 ADC bit = 0.97 mV
MIP peak and S/N Chapter 6.2	with $dE/dx = 11.6 \text{ MeV/cm}$ (measurement by the Dream team with PWO) and 18 cm crystal lenght the MIP peak for Muons lies around 208 MeV	Referring to the MIP peak, the 3 MeV noise leive of a single channel, the Signal/noise level of the FEE electronics is $S/N=70$.
Shaper gain ratio Chapter 8.5	HG/LG design value =16 HG/LG measured =16.83	With the measured gain ratio of 16.83 the dynamic single channel range increases
Sampling rate Chapter 10	Shaper Bandwidth < 0.5 MHz Nyquist frequency 1 MHz 1..20 MHz selectable oversampling @ 10..20 MHz	Readout Bandwith <i>increases</i> with sampling rate Readout Strobe (L1) latency <i>decreases</i> with Sampling rate
Signal sampling latency for Altro strobe L1	$f_S = 10 \text{ MHz}$ $L=1.4 \text{ us}$ after interaction $f_S = 9 \text{ MHz}$ $L=1.26 \text{ us}$ $f_S = 8 \text{ MHz}$ $L=1.12 \text{ us}$	Altro pre-sampling pipline: max. P=14 clocks. With P=14 and level-0 latency L0L =1.4 us, pedestal time is L0L-L.
Samples per event	Max 256 samples + max 15 presamples Typical No of samples 32 or 64	512 available but due to special Altro selection for PHOS, data memory above 256 may contain errors
digitization buffer (MEB)	4 buffers 1024*40 bit or 8 buffers 512*40 bit	with special Altro selection for PHOS, 8 buffers are default
FEE power consumption Chapter 16.2	FEE (32 channel) card 5.2 Watt (add 2 Watt for 32 CSP)	112 FEE cards + 8 TRU PHOS module dissipation ~ 1 kWatt. (add 40m differential LV cable 300 W)
Readout partition	1 RCU and 1 DDL link (Tx, Rx) 2 GTL readout branches 14 FEE and 1 TRU readout branch 2 * 448 channels of 2*10 bit	
Supply voltages and currents Chapter 16	+13.5 V analog, 0.14A -7 V analog, 0.12A +6 V analog 0.32 A analog return 0.73 A digital return 0.45 A +3.3 V analog, 0.34 A +3.3 V digital, 0.31A +4.2 V digital, 0.14 A	LV daisy chain connector Phoenix TMSTBP 2,5/ 8-STF-5,08 +13.5 V-> 12 V Bias + CSP -7 V analog-> -6V shaper,CSP +6 V analog ->5V shaper, Bias +3.3 analog ->1V, 2.5V Altro +3.3 V digital ->2.5V FPGA, Altro, GTL +4.2 V digital ->3.3V Flash, USB, FPGA, Eprom
Fast OR signal shaping Chapter 2.5	Analog Sum of 2*2 crystals FWHM = 100 ns differential	8 way differential, terminated flat cable of 50 cm length, 150 OHM differential, Samtec FFSD-08-D-20.00-01-N Pulsewidth adapted for 4 samples @ 40 MHz in TRU. Max. pulse amplitude of 2.5 V corresponds to 25 GeV
HV Bias input voltage Chapter 2.3	400.0 V +/-0.2V ~0.64 mA for one FEE (32 channels) 7.9 mA for 1 GTL branch (14 FEE)	each FEE channel ~ 20 uA. Note: above 400V protection starts shunting current !
APD Bias regulation Chapter 2.3	10 bit between 210-400 V (~ 0.2 V per bit)	Regulation of 32 HV channels via 32 DAC registers in PCM controller, no direct HV readback possible

Table 3 Offline evaluation with testbeam data

Observable	value	Remarks
Energy resolution σ/E Chapter 1.3	Fit values with old electronics 2002-2004: $a_{\text{noise}} = 13 \pm 0.7 \text{ MeV}$ $b_{\text{stochastic}} = 0.0358 \pm 0.002 \text{ (3.58 \% GeV}^{0.5} \text{)}$ $c_{\text{const}} = 0.0112 \pm 0.003 \text{ (1.12 \%)}$ New prelim. testbeam 2006 with FEE electronics: $a \sim 10 \text{ MeV}$, $b = 2.8\%$ and $c = 0.8 \%$	valid for 3*3 crystal cells
Timing resolution (differential) Chapter 5	Not yet available with particles	

1 PHOS basics

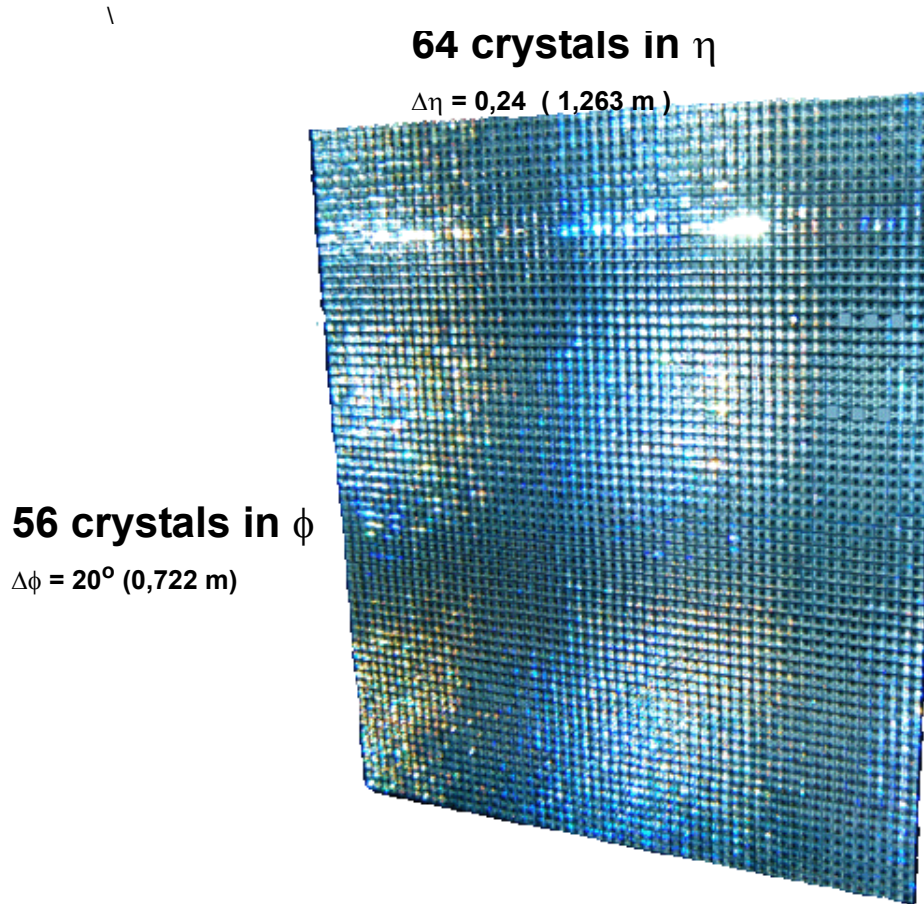


Figure 1 Photo of 1 PHOS Module with $56 \times 64 = 3584$ PWO crystals

1.1 Electromagnetic showers in PbWO_4

The energy of an electromagnetic particle is converted inside the dense PbWO_4 crystals into showers of electrons and photons. This is due to Bremsstrahlung of electrons which yield photons and due to photon pair production which yields electrons and positrons. The length of this repetitive shower process is characterized by the radiation length X_0 of the material, a property which is related to the mean free path of a photon, before it produces a pair by $X_p = 9/7 X_0$. The PHOS crystals represent 20 radiation length, hence the energy of an

incident photon is split into a very large number photons and electrons with their energy absorbed over 20 radiation length until the critical Energy E_c (8.5 MeV) is reached and the ionizing processes (compton and photoeffect) prevail and produce the scintillation light (2.9 and 2.5 eV). The longitudinal EM shower maximum [28] in radiation length is at

$$t_{\max} = \ln\left(\frac{E_0}{E_c} \cdot \frac{1}{\ln 2}\right)$$

The 95% containment is at $t_{\max} + 9.6 + 0.08Z$ i.e. for a primary photon with $E_0=10$ GeV, the shower maximum is at ~ 7.4 radiation length (6 cm) and 95 % is at ~ 20 radiation length (18 cm). The leakage of energy below 10 GeV is still less than 5 %. With increasing energy E_0 however the energy signal measured by PHOS must be offline corrected for the leakage.

The transverse shower development is measured by the Moliere Radius in which 95% of the shower are

$$R_M = \frac{21\text{MeV}}{E_c} \cdot X_0 \cdot \left[\text{g/cm}^2 \right]$$

contained. With $R_M = 2$ cm for a crystal dimension of 2.2×2.2 cm along the shower, more than 90% of the showers are contained in quadratic crystal patches of 2×2 crystals of 18 cm length.

1.2 Shower-sums

Electromagnetic showers extend over several crystals such that a centrally hit crystal is concerned by ca. 80% of the shower, hence the 100% particle energy is only obtained by summing over neighboring crystals. The energy reconstruction is done in PHOS offline by summing over 3×3 quadratic crystal patches like in Figure 2, which altogether contain the almost full shower information. The offline summing is based on the digital measurement produced by each channel.

Energy, energy resolution and noise are therefore referenced to 3×3 crystal areas.

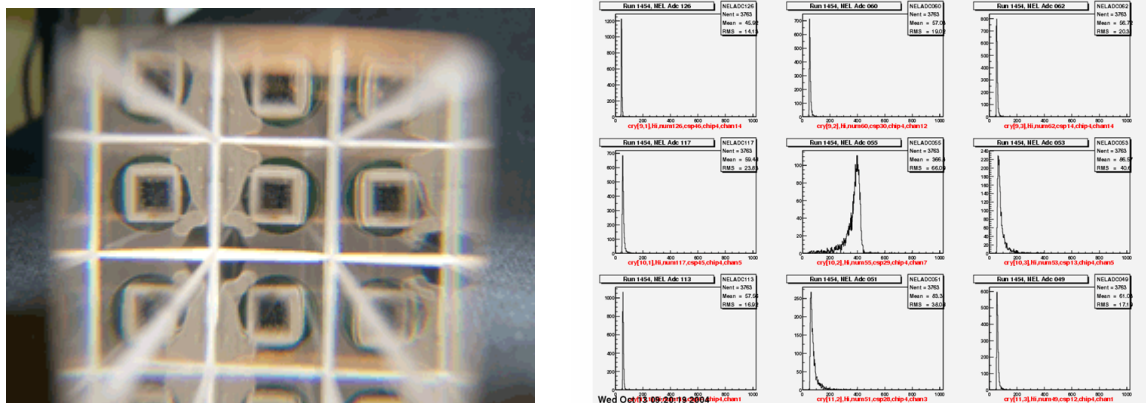


Figure 2 Left side: Photo of a 3×3 crystal region of PHOS. The APD diodes are visible at the far end though the crystal. Right side: the corresponding offline shower energy distribution in each crystal for a central (slightly off-center) electron of 2 GeV.

A more quantified measurement with a cosmic electron shower recorded with PHOS is shown in Figure 3

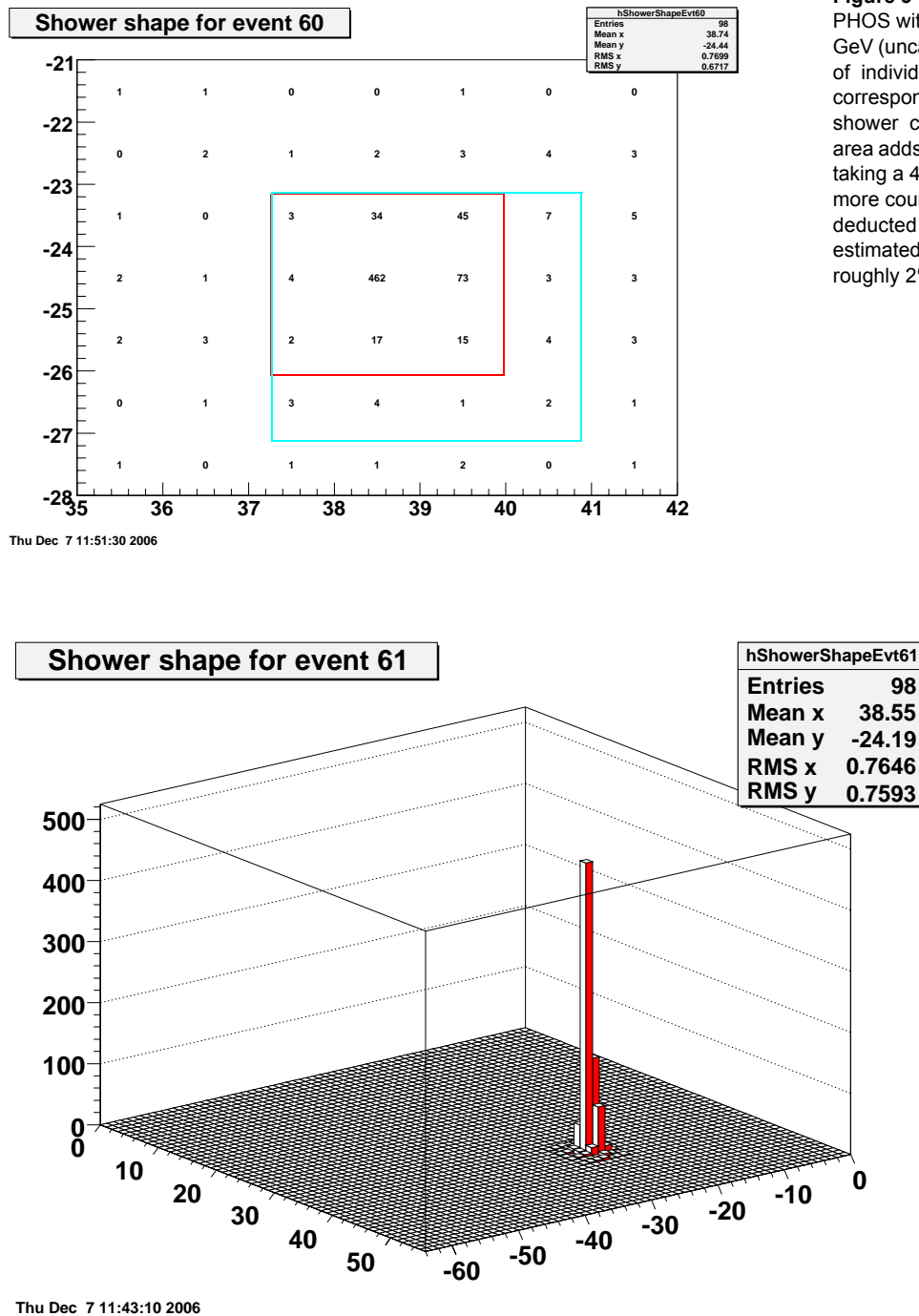


Figure 3 Cosmic electron shower in PHOS with a particle energy of ca 3 GeV (uncalibrated) Top: ADC counts of individual crystal cells. Bottom: corresponding Lego plot. The shower contained in the framed 3x3 area adds up to 655 ADC counts. By taking a 4x4 area there would be 24 more counts of which 6 can be deducted as background. Hence the estimated containment in 4x4 is roughly 2% more than in 3x3.

which indicates that the 3x3 sum contains ca. 97% of the shower.

The pulse representation of an electromagnetic shower is depicted in Figure 4

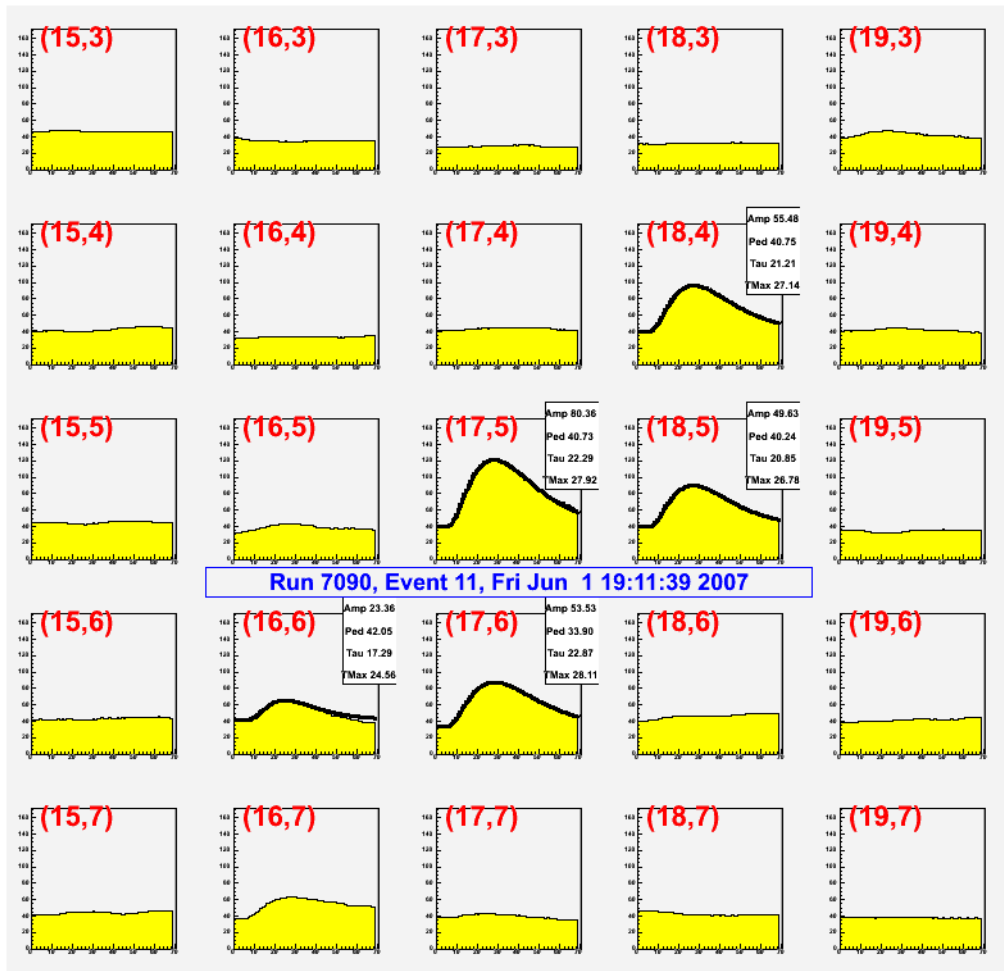


Figure 4 Electromagnetic (cosmic) shower, viewed in the time domain in 5 x 5 crystals . The bold black lines indicate the signals where the semi-gaussian (Gamma-2) fit was successful.

1.3 Energy resolution

The PHOS energy resolution σ/E as function of energy was measured [19] with a 16*16 PHOS prototype matrix during the PHOS testbeams 2002 ... 2004 and later with the first PHOS module in 2006 [30].

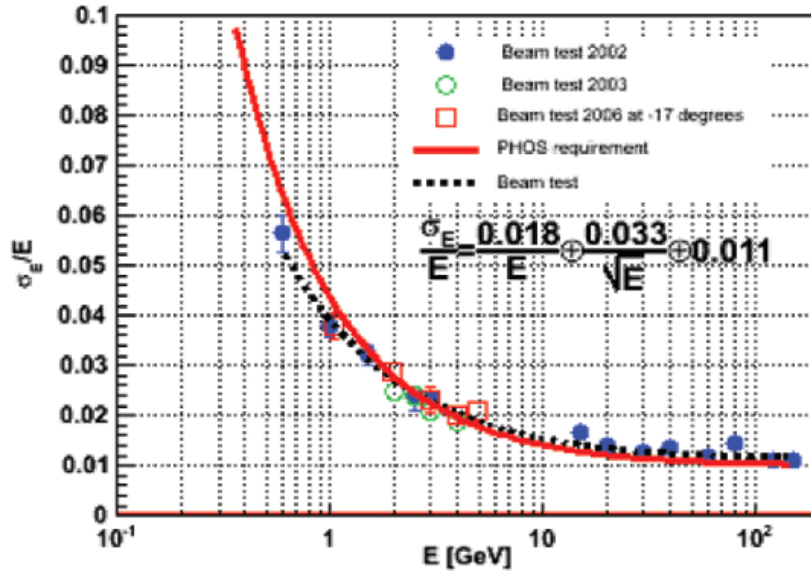


Figure 5 Testbeam Results 2002-2006 of PHOS energy resolution. The measured resolutions match with the requirement (red line).

The σ/E dependence was fitted with the standard parametrization for calorimeters (Equation 1) using 3 constants a , b and c that can be derived from the fit to the testbeam data.

$$\frac{\sigma}{E} = \sqrt{\frac{a^2}{E^2} + \frac{b^2}{E} + c^2}$$

Equation 1 Standard parameterization of calorimeter energy resolution

The noise term “a” dominates in the low energy range. It is due to electronics noise, generated by parallel and serial noise sources at the capacitance of the APD and the CSP input (J- FET), both due to APD dark current and the noise voltage at the FET of the preamplifier. Other contributions like pileup and radioactivity are negligible for PHOS. The energy resolution and noise term apply to the active volume of a shower, hence to 3*3 crystals. The 3x3 noise is added under the square-root, and is therefore given as three times the single-channel noise.

The stochastic term “b” is the dominant term in mid-to-high energy ranges, allowing to characterize calorimeter resolution as $\sigma/E = b/\sqrt{E} \oplus c$. The stochastic term b is due to statistical effects of shower fluctuations and due to APD excess noise.

The constant term “c” limits the energy resolution in all energy ranges and is given by quality and detection losses of the calorimeter. In particular inter-calibration, non uniformities, non-linearities, instabilities in temperature and high voltage, as well as rear/front light leakage contribute directly to the constant term.

The preliminary determination of coefficients from the fit to the data of Figure 5 with 2003 and 2004 test beam data [31] with old electronics gave the following values:

- $a_{\text{noise}} = 13 \pm 0.7 \text{ MeV}$
- $b_{\text{stochastic}} = 0.0358 \pm 0.002 \text{ (3.58 \% GeV}^{0.5} \text{)}$
- $c_{\text{const}} = 0.0112 \pm 0.003 \text{ (1.12 \%)}$

Figure 6 shows a new fit on the combined testbeam data 2002-2006 with $b/\sqrt{E} \oplus c$. The square points represent data taken with new FEE electronics. At low energy ($1/\sqrt{E} > 1.3$ or below 600 MeV) the noise term starts to dominate as shown by the old 2002 testbeam point in the middle, which was taken with old electronics. With the new FEE electronics, available first time in the 2006 testbeam (square points), the noise-term is less. Minimum ionizing muons (MIP point) are resolved¹ with only moderate deviation from the b/\sqrt{E} slope at ca. 210 MeV.

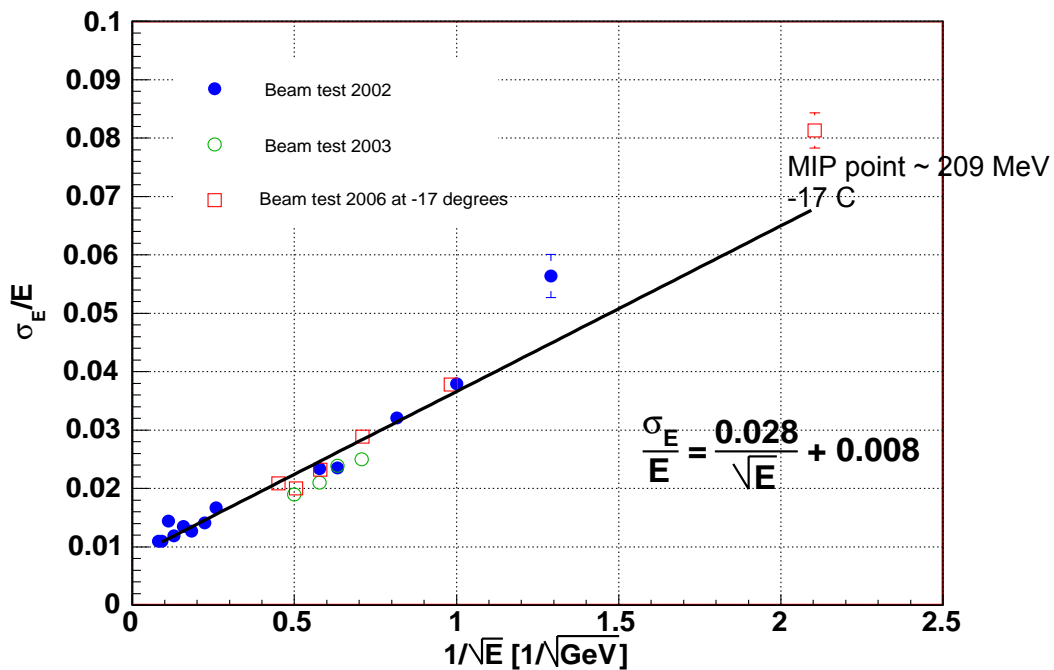


Figure 6 PHOS testbeam data fit of testbeam data 2002-2006 with $1/\sqrt{E} \oplus c$

The fit constants with new data are with $b = 2.8\%$ and $c = 0.8\%$ slightly improved.

1. since MIP muons are not producing showers this point is representative only for a single crystal whilst all other points represent energy measured in 3x3

1.4 Dynamic range

Two 10 bit digitization ranges per channel are combined in the FEE card electronics with two different amplification gains. Taken together, the high and low gain channels cover a dynamic range of 14 bit. Figure 64 shows that the shaper signal is split into 2 shaper/ADC channels with different gains of design value 2×3.25 and 2×0.2 . Based on the 10 bit range of each ADC, the design value of the overlapping total dynamic range is 14 bit¹.

The offline gain ratio per FEE channel was measured (chapter 8.5) showing a very good uniformity. The offline measured gain ratio, taken with a LED pulser² and APD at -25°C is 16.83 (see chapter 8.5). The measured ratio is slightly higher from the design value, leading to an effective increase of the targeted dynamic range.

The two gain ranges of a single FEE channel³ cover a total 14 bit design range between 5 MeV and 80 GeV. For electromagnetic particles which are distributed over a 3×3 crystal range this corresponds to a 20% higher range from 5 MeV to ~ 100 GeV. As shown in Figure 7, the single channel digital resolution (ADC-count/1024) lies (apart from the 5 GeV crossover point) well below the requirement of the PHOS I calorimeter.

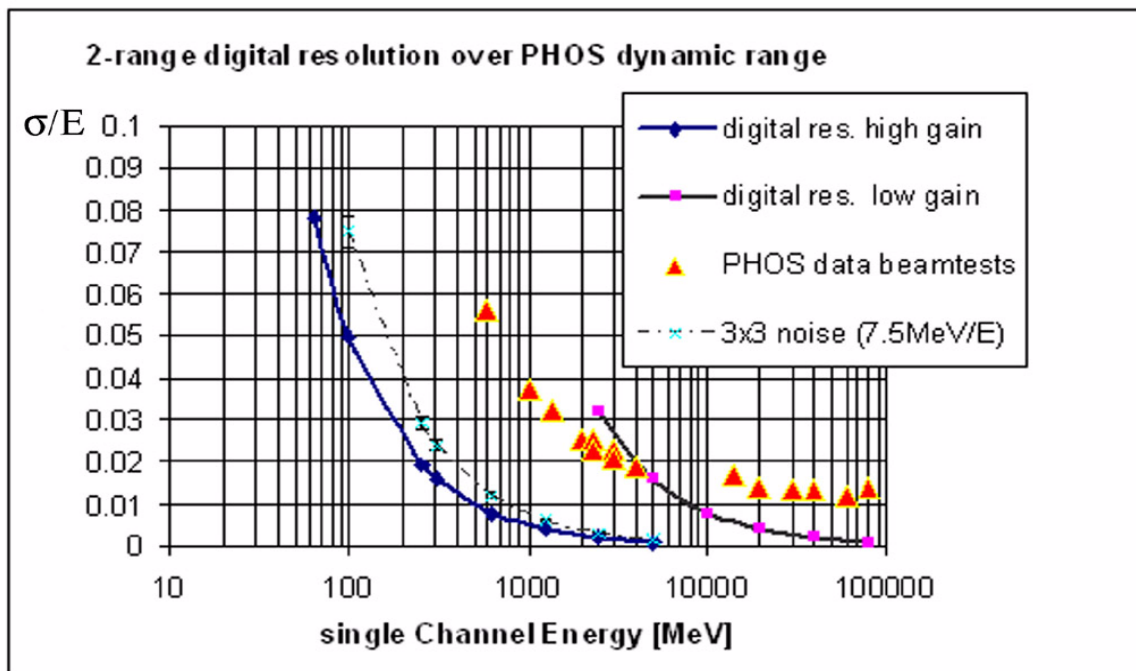


Figure 7 two-range single channel digital resolution compared with test beam data and 3×3 noise

The crossover between low and high gain digital resolution lies at 5 GeV for a nominal APD gain of $M=50$ and a shaper gain ratio of 16.0. The combined resolution is slightly worse above 5 GeV but still below the required resolution as indicated by the data points.

1. with 10 bit single range and a gain ratio of $\sim 16 = 2^{4.0}$ the effective range is $10 + 4 = 14$ bit

2. the same measurement taken with step pulser gives ca 10% higher ratio due to the pole zero-overcompensation with artificial step pulsers

3. The range selection was chosen starting from the requirement that 100 GeV central photons correspond to ca. 80 GeV deposited energy in a single crystal. By selecting 80 GeV as the maximum 10 bit value of the high energy digitizer, the digital resolution near 5 GeV is equal to the energy resolution, hence the maximum 10 bit value of the low energy range is set to 5 GeV as crossover point for the two ranges. Based on this, the LSB setting for the digital channel resolution corresponds to 5 MeV which is above the single channel RMS noise floor of 1...3 MeV.

The dynamic range of a single channel for a shaper gain ratio of 16.0 would be $80 \text{ GeV} / 5 \text{ MeV} = 2^{14}$ (= 14 bit). With the 3x3 energy range up to 100 GeV, the dynamic range is slightly more than 14 bit (~14.3 bit)

The effective dynamic range of a single channel for the measured gain ratio 16.83 (see chapt. 8.5) is

$$5 \text{ MeV to } 86.16 \text{ GeV.}$$

The dynamic range scales with the energy equivalent which is chosen for 1 ADC bit. Different crystal light yields, different temperatures allow to select different energy equivalents for 1 ADC count by varying the APD gains.

Note: The assumption for this document is that the three variables are in a constant relation such that 1 ADC count is equivalent to 5 GeV.

1.5 Timing resolution

The PHOS detector requires a very high timing resolution in order to determine, via Time of Flight (TOF) measurements, whether events are of electromagnetic nature or produced by thermal neutron + anti-neutron annihilation. The latter are produced in the energy range between 2 to 4 GeV. The percentage of n/γ contamination in this energy range can reach 30%. A large part of the contamination can be discriminated by the sphericity factor of the shower shape for gammas and hadrons (see chapter 4.6 in [1]). With additional TOF measurements, the contamination can be reduced to a few percent for a systematic error of a few percent. The simulation

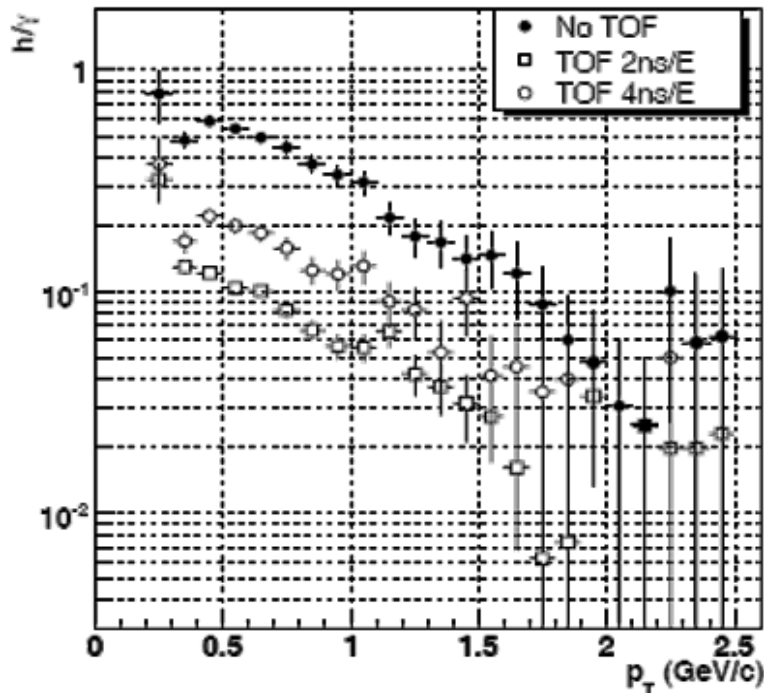


Figure 8 Ratio of n/γ contamination fraction as function of transverse momentum for different TOF cuts. Source Yuri Kharlov, presented in [30]

shown in Figure 8 indicates that a TOF resolution of 1 ns at 2 GeV reduces the n/γ contamination by a factor of 2 compared to a TOF resolution of 2 ns.

The following factors limit the timing resolution of PHOS:

- The intrinsic timing resolution of PWO crystals (measured with Photomultipliers [32]) is 130 ps.
- The timing resolution with APDs, measured in a PHOS testbeam in June 2004 with a high-resolution TDC (Figure 9) is constant ~ 500 ps above 1.5 GeV. (Note that the timing resolution is energy dependent only in the low resolution region of the TDC)
- The timing resolution of FEE electronics alone (measured with a step pulser) is ~ 0.5 ns at 1 GeV (see chapter 28.4)

The combined timing resolution with FEE electronics is limited to ca. 1 ns at 1 GeV.

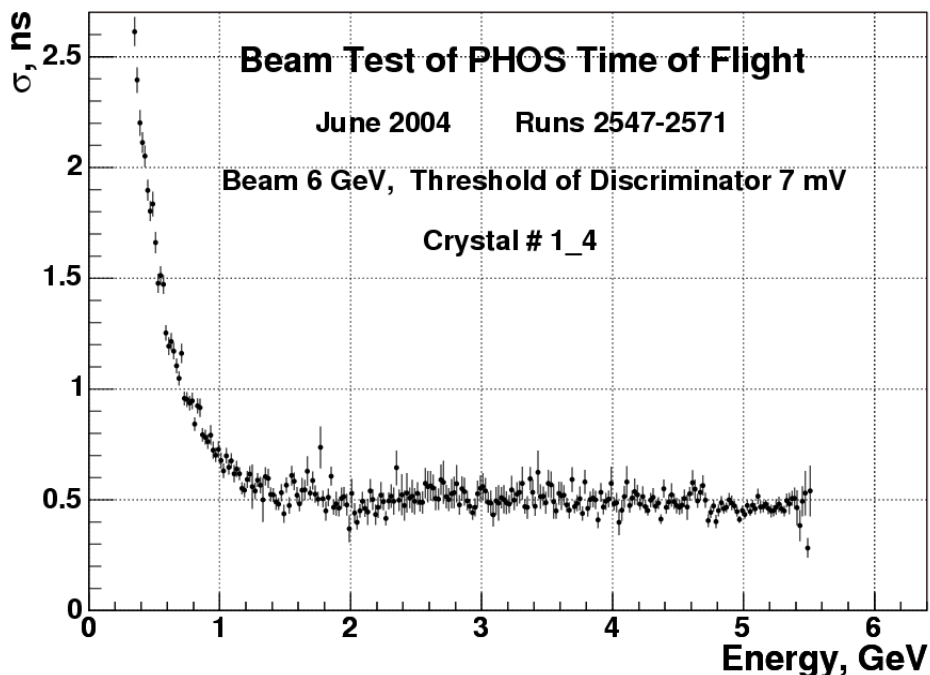


Figure 9 Timing resolution of PWO/APD measured with a precision TDC in June 2004 testbeam. There is no energy dependence above 1 GeV.

The PHOS FEE electronics does not contain hardware TDC logic¹ since it was decided very early on to derive timing information from the offline shape of the energy pulse.

The shapers of the FEE card are designed to reproduce a Gamma-2 function which has two amplitude-independent time reference points at its first derivative (max. amplitude) and second derivative (slope change in pulse risetime), see Figure 41.

1. The addition of TDC channels to the FEE would have significantly increased complexity and power at reduced channel density and significantly higher cost.

The timing resolution which has been determined offline from the FEE shaper pulse (Figure 10) shows a strong energy dependence which is due to the limited number ADC bits¹ available on the FEE cards to measure the particle energy E: there are only 400 of 1024 ADC counts available at 2 GeV, or 200 at 1 GeV. which means the digital resolution effectively drops with 1/E.

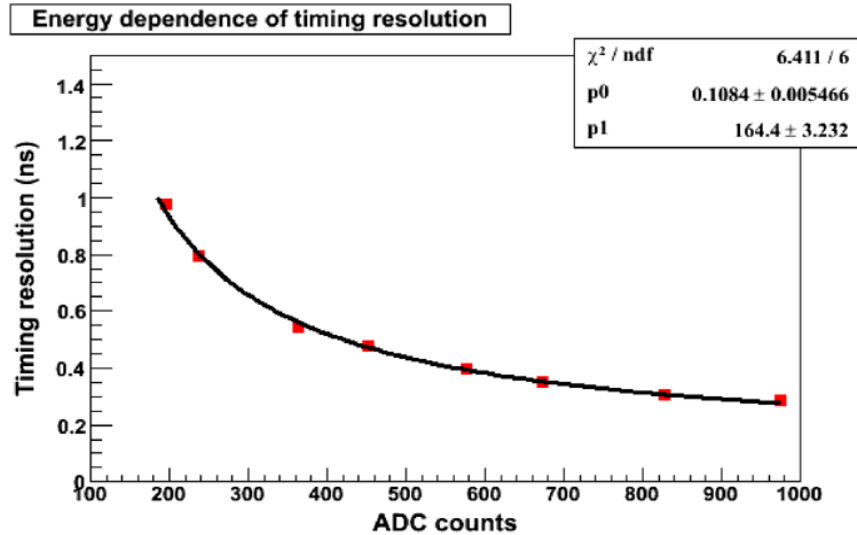


Figure 10 Measured energy dependence of timing resolution of FEE electronics for test pulses generated with a step pulser at the input of the FEE electronics. At 400 ADC counts (= 2 GeV) the FEE timing resolution for artificial step pulsers is ca 500 ps.

1. the number of bits available at 1 GeV are 400 ADC counts out of 1024. More ADC bits could only be gained by changing the 5 MeV equivalent for 1 ADC count, which would however change the dynamic range.

1.6 Timing resolution as function of ADC sampling frequency

The timing resolution, measured offline from the shaper pulse is a function of the sampling frequency. In view that the -10dB signal bandwidth point is ca. 500 kHz for a shaping time of 1 μ s¹, the Nyquist theorem says that (over)sampling above twice the 500 kHz bandwidth does not add information. The timing resolution measurement [34] of Figure 11, taken with a 1 ns risetime blue LED pulser and at an APD temperature of -25 C demonstrates that the timing resolution, obtained by a fit on the offline pulseshape, remains indeed constant above 1 MHz at ca 1.45 ns for 400 ADC count signals (this corresponds to 2 GeV for a calorimeter calibration of 5 MeV/ADC count.)

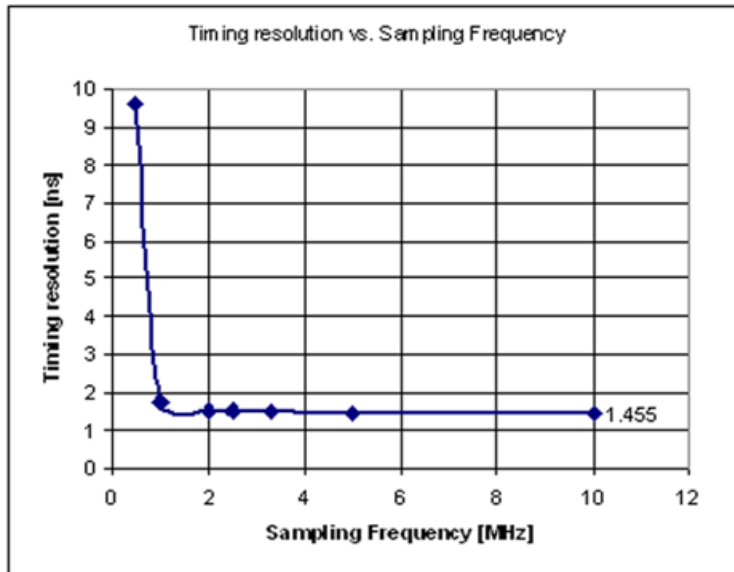


Figure 11 Timing resolution as function of the ADC sampling frequency, measured with a LED pulser

1.7 PWO crystals

The natural form of synthetically grown PbWO_4 crystals is the Stolizite, a crystal of quadratic and bi-pyramidal structure with natural colors: yellow, red, brown. The other natural form of PbWO_4 is Raspite, however its different crystal structure turns into Stolizite when heated above 400 C. The industrial production of Apatity synthetic PWO crystals for PHOS is based on the Czochraski method: Two metallic oxides PbO and WO_3 , powders of very high purity, are mixed in proportion 1:1 and heated to the melting point i.e. above 1123 degree C. An original crystal seed is then inserted and rotated at ca. 15 rotations /minute and pulled out vertically at 5mm /hour. After ca. 60 ..75 hours, a round crystal of ca 25 cm length is grown (see Figure 12). In a subsequent annealing process, the crystals are re-heated in specifically chosen atmospheres in which transparency and colors are optimized.

1. 1 μ s shaping time means that at above center frequency of $f_c = 1\mu\text{s}/2\pi = 160$ kHz the 2nd order shaper bandpass attenuates the signal by -40 db per 10x frequency interval

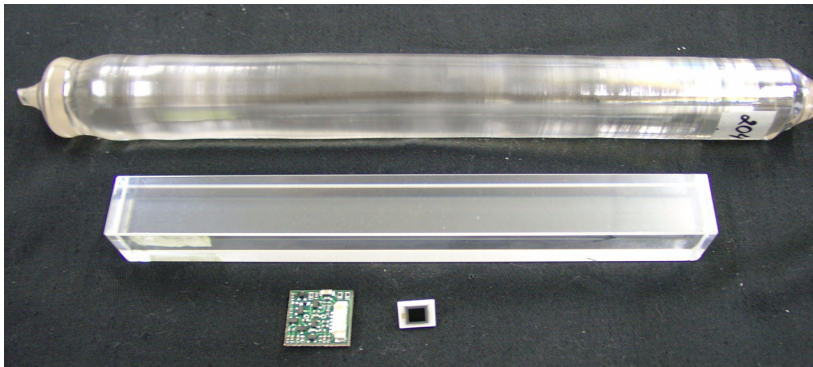


Figure 12 PWO crystals: Top: synthetic raw crystal Middle: rectangular cut-out crystal after polishment Bottom: comparative size of 5x5 mm² APD and preamplifier.

1.8 PbWO₄ properties

The electromagnetic PHOS calorimeter is constructed from synthetically manufactured, inorganic PbWO₄ crystals (short: PWO) which are fast scintillators of relatively low light-yield and short radiation length. These crystals emit mainly two spectral lines: 420 nm (blue) and 480 -520 nm (green) with decay times in the order of 10 ns. With a radiation length $X_0 = 0.89$ cm, the PWO crystal has a Moliere radius of 2 cm for 95% transverse electromagnetic shower distribution. The incident photon angle per crystal is smaller than ± 13 degrees. Each crystal has a size of 22* 22 * 180 mm³ of which 180 mm (equivalent to $\sim 20 X_0$) was chosen as a compromise in price and absorption efficiency of electromagnetic showers, for optimal energy resolutions up to 10 GeV. The properties of PWO crystals are summarized in Table 1 :

Table 1 PbWO₄ crystal properties (synthetic Apatity production >2004)

Density	8.28 g/cm ³	(compare: Pb =11.35g/cm ³)
Radiation length X_0	0.89 cm 7.37 g/cm ²	approx. conversion length via process $e^- \rightarrow 2\gamma$, or $\gamma \rightarrow e^+ e^-$
Moliere Radius R_M	2 cm	95 % of shower cone located in a cylinder with radius R_M
dE/dx for cosmic MIP (muons)	11.4 MeV/cm [33]	cosmic muons through 18 cm PWO leave 205 MeV
interaction length	19.5 cm	
critical Energy E_c	8.5 MeV	Radiation region $E > E_c$
Decay time	10.6 ns (Figure 20	room temperature
Peak emission	420 (f) nm = 2.9 eV (blue) 480-520(s) nm =2.5 eV (green)	f =fast component, s=slow component
refractive index	2.16	along z (ζ axis)
light output	10 - 12 pe / MeV	improving per production year
hygroscopy	no	
melting point	1123° C	

The optical properties of the PHOS crystals are depicted in Figure 13 and Figure 14 below. Wavelengths above 370 nm are uniformly transmitted. The APD quantum efficiency is > 50% above 370 nm (see Figure 17).

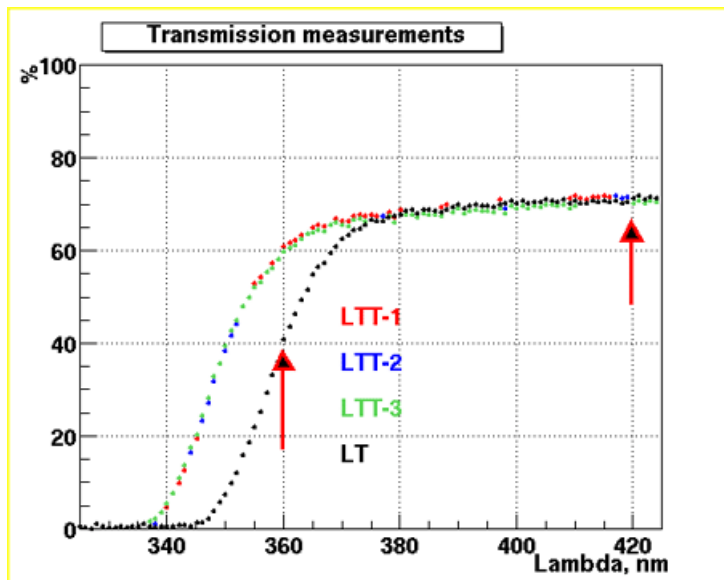


Figure 13 PWO transparency as function of wavelength

The maximum wavelength of the PWO emission spectrum is 440 nm. .

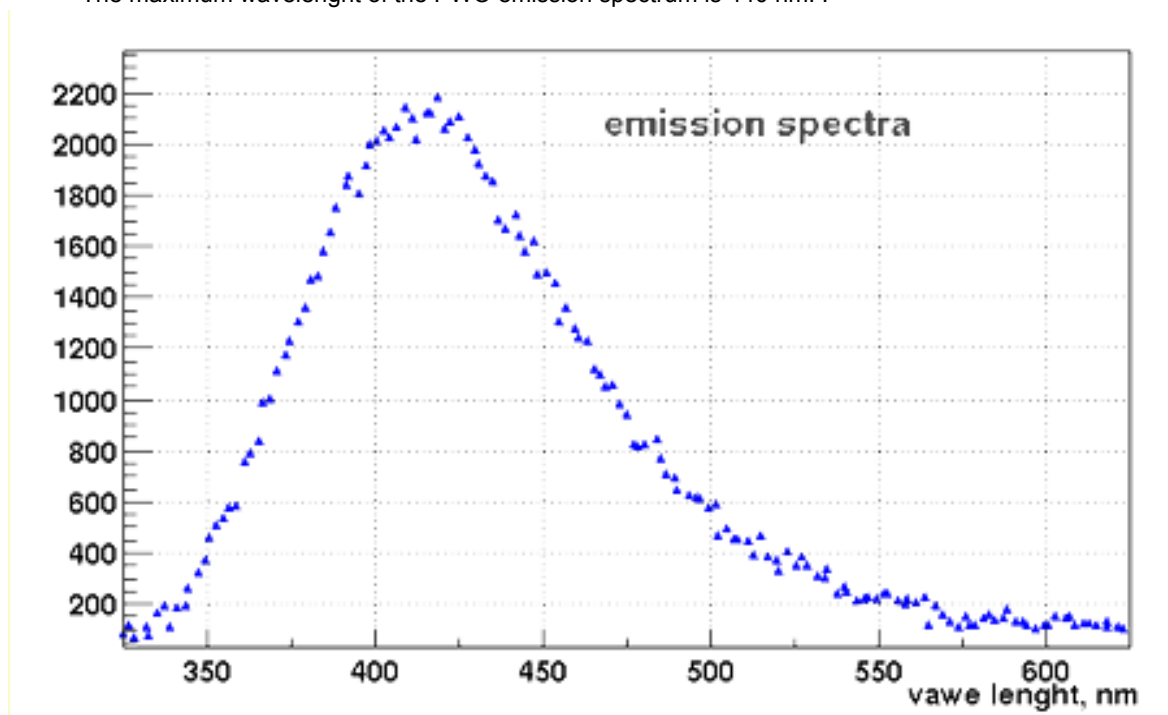


Figure 14 Emission spectrum of one PW crystal

1.9 Conversion wavelenght - electron volt- visible light

Since $1\text{eV} = 1.6 \times 10^{-19}$ Coulomb x Volt (Joule) the conversion in wavelenght goes via $E = h\nu$ where $h = 6.626 \times 10^{-34}$ Js is the Planck constant and $\nu = 1/T = c/\lambda$ where $c = 3 \times 10^8$ m/s is the speed of light and λ the wavelenght in meters

Hence

$E[\text{Joule}] = c \cdot h / \lambda [\text{m}]$ and $E(\text{eV})$:

$$E(\text{eV}) = \frac{hc}{\lambda} = \frac{(6.626 \times 10^{-34}) \cdot (3 \times 10^8)}{\lambda(\text{nm}) \cdot 10^{-9} \cdot (1.6022 \times 10^{-19})} = \frac{1240}{\lambda(\text{nm})}$$

The relation is depicted in Figure 15 with indication of the visible light between 1.8 and 3.1 eV.

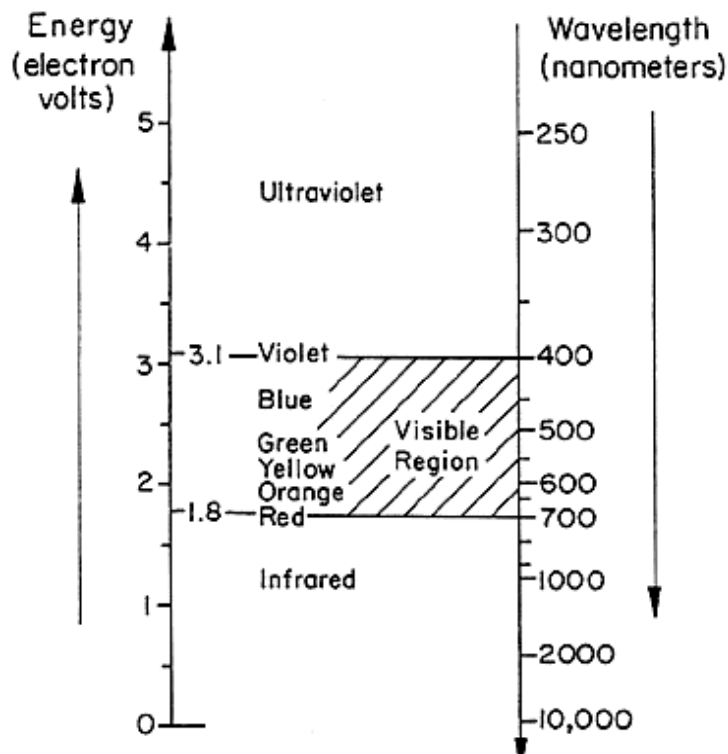


Figure 15 Conversion of light wavelength into electron volt

1.10 Light Yield

The light yield of a crystal is measured by a photomultiplier as number of photoelectrons per energy unit. The average light yield for PWO crystals is characterized by annual improvement between competitors¹ being a function of crystal growing axis and of annealing and doping.

The manufacturing quality for PHOS crystals in North Russia (Apatity) improved from 7 to 12 e-/MeV from 2001-2006. Since the light yield for PWO is a strong function of temperature [1] and roughly a factor 3 higher at -25 °C than at 25 °C [Figure 16], it was decided to operate PHOS at -25 °C in order to have the same amount of photo-electrons per MEV as with several APDs at room temperature. .

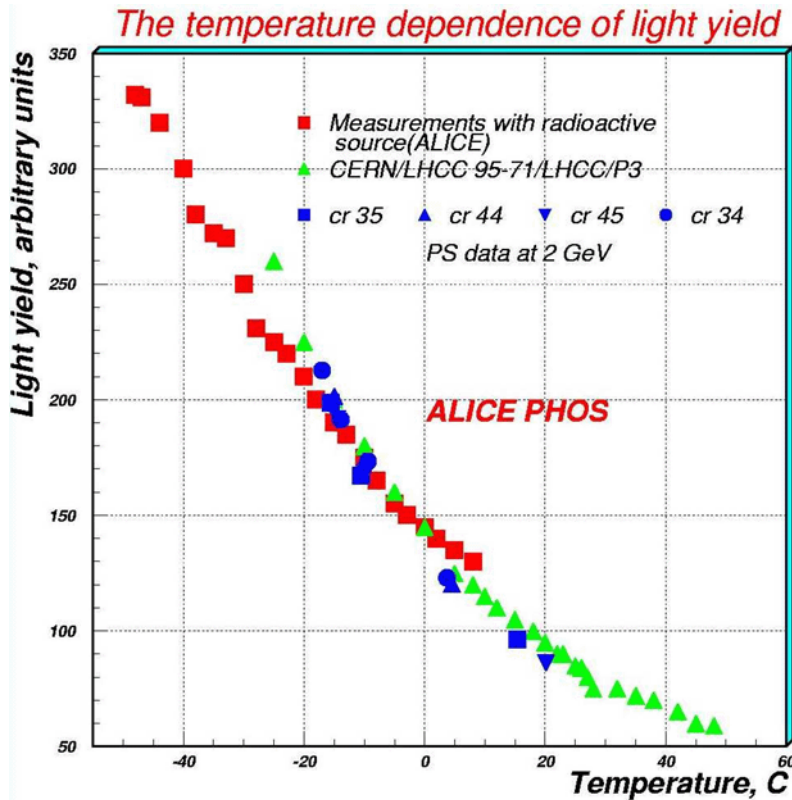


Figure 16 Light yield dependence on temperature [1]

Whilst precision light measurements are best obtained with photomultipliers which have single photoelectron resolution, PHOS has chosen for cost, complexity and space reasons to use avalanche photo diodes (APD) with a signal over noise level of ca. 10 photoelectrons. The light yield measured of PM's needs correspondingly be corrected for APD detectors.

The light yield of the PHOS crystals is nominally $LY = 10 \text{ pe/MeV}$, measured by XP 2262b at room temperature at a quantum efficiency of 25%. In order to obtain the light yield with APD's, the sensitive areas PM / APD and the quantum efficiencies of PM / APD must be taken into proportion.

1. PWO manufacturers: a.) North Crystals Company, Apatity, Murmansk Region, Russia. (Alice PHOS $22 \times 22 \times 180 \text{ mm}^3$ b.) BCTP, Bogoroditsk, Russia (CMS Ecal $28.52 \times 220 \times 30.02 \text{ mm}$) c.) SICCA, Shanghai Institute of Ceramics, Shanghai, China, (PrimEX $22 \times 22 \times 230$)

1.10.1 Light yield with APD diode

The APD's and the following FEE electronics measure the charge signal produced by the scintillation light. The number of electrons N_{APD} produced by an APD by a 1MeV electromagnetic particle in the PWO crystal at temperature 25°C at APD gain $M=1$ can be estimated by comparing with the PWO light yield measurements taken with a photomultiplier which covers the PWO full exit window. For average PWO crystals with light yield $=10$, one obtains for blue light of 420 nm wavelength, by putting detector surfaces and quantum efficiencies in relation:

$$N_{APD} = N_{PMT} \times (S_{APD}/S_{PMT}) \times (E_{APD}/E_{PMT})$$

$$= 10 \times (25/484) \times (0.7/0.25) = \underline{1.45e/MeV} \quad (LY=10, +25^\circ C)$$

Where:

- N_{APD} - quantity of electrons in APD;
- N_{PMT} - quantity of electrons in PMT;
- S_{APD} - area of APD S8148 (5 * 5 mm²)
- $S_{PMT} = S_{PWO}$ area of PMT covered by the PWO window 22 * 22 mm²
- E_{APD} - quantum efficiency S8148 @ $\lambda=420$ nm ($M=1$) = 70 %
- E_{PMT} - quantum efficiency EMI 9814b @ $\lambda=420$ nm = 25 %
-

■ Quantum efficiency vs. wavelength

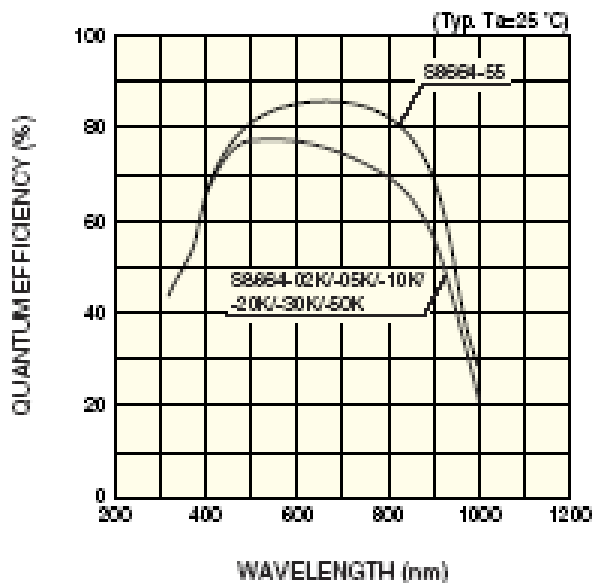


Figure 17 Quantum efficiency of APD in dependence of wavelength. The Hamamatsu APD S8148 is equivalent to S8664-55. For 420 nm, the quantum efficiency is 70 %

At -25°C the PWO light yield increases by a factor between 2.5 to 3. (see Figure 16) We interpolate the temperature factor to 2.75.

$$N_{APD}(-25^{\circ}\text{C}, M=1) / \text{MeV} = 2.75 \times N_{APD}(+25^{\circ}\text{C}, M=1) \sim 4 \text{ e}^{-}/\text{MeV}$$

Equation 2 Photoelectrons per MeV for a crystal with LY=10 @ -25 °C

With the above, the CSP preamplifier voltage step for 1 MeV showers with an APD gain M and feedback capacitor $C_f=1.2\text{pF}$ is equal to Q/C_f ; hence with $e=1.6 \cdot 10^{-19}$ Coulomb

$$U_{\text{csp}}/E|_{V/(\text{MeV})} = M \cdot N_{\text{apd}} \cdot e / C_f = M \cdot 0.533 \cdot (\mu\text{V})/(\text{MeV})$$

Equation 3 CSP output Voltage per MeV @ -25 C

By including the CSP's intrinsic ENC noise of 520 electrons for a detector capacitance of 100 pF, this becomes

$$U_{\text{csp}}/E = \lfloor M \cdot 4/(\text{MeV}) + 520 \rfloor \cdot e / C_f = \lfloor 0.533 \cdot M/(\text{MeV}) + 69 \rfloor (\mu\text{V})/(\text{MeV})$$

Equation 4 CSP output Voltage per MeV including ENC

The corresponding CSP output Voltage per MeV as function of the APD gain M is shown graphically in Figure 18

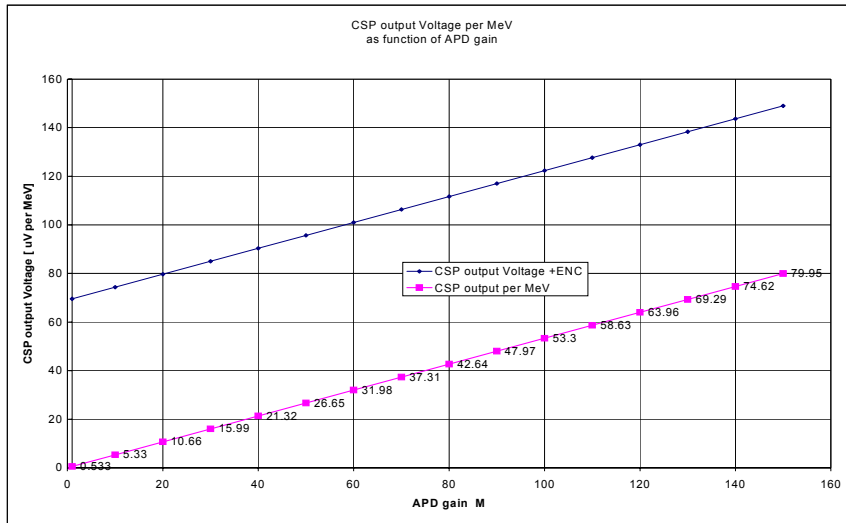


Figure 18 CSP output Voltage as function of APD gain in uVolt per MeV for crystals with a nominal Light Yield of 10. The CSP's intrinsic ENC is a constant offset (69 uV).

For M=50, the relevant figure for signals far above noise is 26.7 uV / MeV

With a nominal APD gain choice for PHOS of M=50, the APD charge signal is:

$$N_{\text{PHOS-APD}}(-25^{\circ}\text{C}, M=50) \sim 220 \text{ e}^{-}/\text{MeV}$$

The light-to-charge conversion of an APD diode generates a charge signal Q which is proportional to the scintillation light which is, when integrated over the shower size, proportional to the energy E of the initial particle. With an electron charge of $e=1.6 \cdot 10^{-19}$ Coulomb and an APD gain M [see chap 2.1.1] which increases with the reverse bias voltage, the charge signal is

$$Q = N_{APD(-25\text{ C})} * M * e * E [\text{MeV}]$$

This charge signal Q is converted into a step voltage over the charge capacitor C_f (1.2pF) of the Charge Sensitive Preamplifier (CSP) with amplitude $U = Q / C_f$ (see chapter 3) and the corresponding voltage signal at the preamplifier output is

$$U_{\text{CSP}} = 26.7 \text{ uV / MeV}$$

for PWO crystals with LY=10 at -25° and for nominal APD gain $M=50$.

1.10.2 Timing of PWO scintillation light

The PWO emission spectrum consists of a blue light component with maximum at 420 nm and a green component with maximum at 500 nm. After 2...5 ns risetime, the luminescent intensity decreases rapidly by two orders of magnitude. The decay can be described as superposition of several (4) exponential decay components of different amplitudes and decay constants of which the fastest is 2...3 ns and accounts for 20-30% of the light yield. $F(x)=P1\exp(-x/P2)+P3\exp(-x/P4)+P5\exp(-x/P6)+P7$ which is fitted Globally, after 40 ns only a very small fraction of the initial luminescence is still observable.

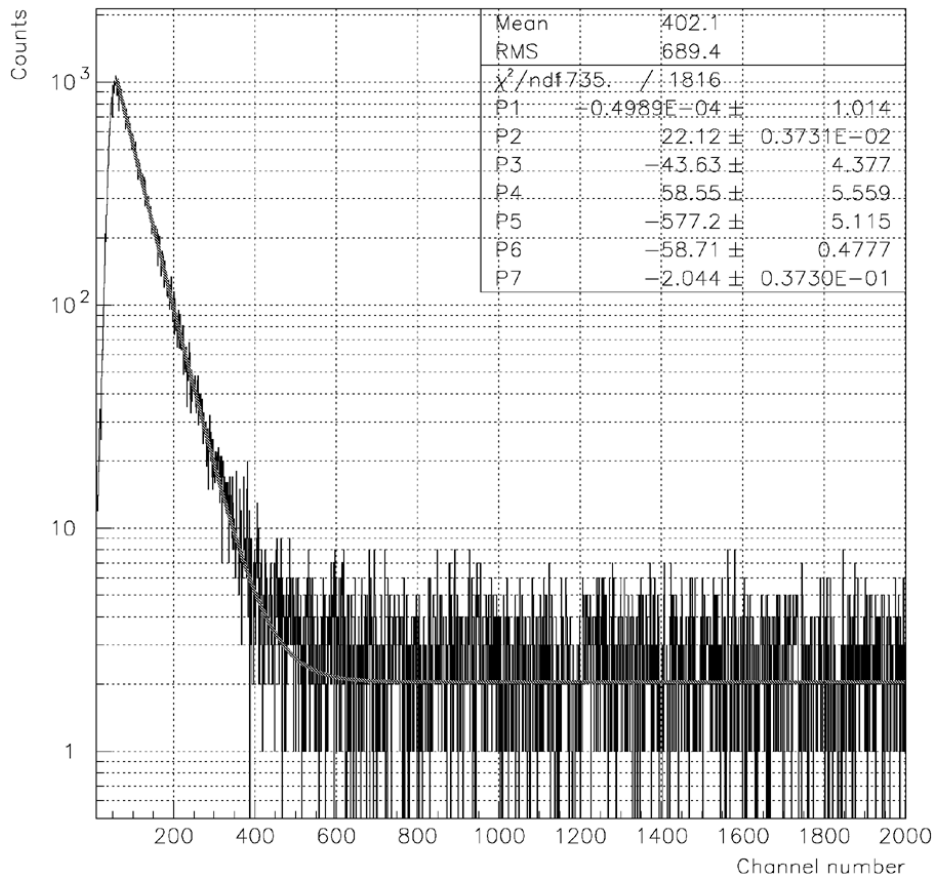


Figure 19 Decay time measurement of PWO crystal

The decay time is normally measured at room temperature, with lower temperature, the total luminescence decay time gets slower (ca. 20 ns per 25 Kelvin).

The APD charge integration by the CSP can be approximated by the integral over a $\delta(t)$ charge input function, giving as result an ideal step output. The $\delta(t)$ charge is however only an approximation and has to be replaced by a charge generation process consisting of several time-constants. The observable effect is that the CSP output risetime is composed of several slopes and the peaking time of the semi-gaussian output pulse is delayed by the amount of the risetime delay of the input signal. In view that the peaking time of the semi-gaussian is 2 μ s, the constant shift by a few ns is irrelevant.

1.10.3 Cerenkov light in PWO crystals

With a PbWO_4 refractive index of $n=2.16$ along the z axis, there is also a certain amount of prompt Cerenkov light produced in the crystals when a charged particle passes with velocity in an emission cone of which the

$$\beta \geq \beta_{\text{thresh}} = \frac{1}{n}$$

saturated emission angle is Θ_{max} . Using a PWO crystals¹ with $\Theta_{\text{max}}=63^\circ$, the fraction of Cerenkov light has

$$\Theta_{\text{max}} = \arccos \frac{1}{n}$$

been measured [33] with muons at room temperature as ca 17%. The prompt nature of the Cerenkov light compared to Scintillation light could in principle be detected by very fast electronics which can resolve a difference of 1 ns. With APDs and a charge sensitive preamplifier, the prompt Cerenkov signal contribution to risetime of the CSP step voltage is hardly distinguishable. The time structure of the signal Landau tail shows 10.6 ns decay time.

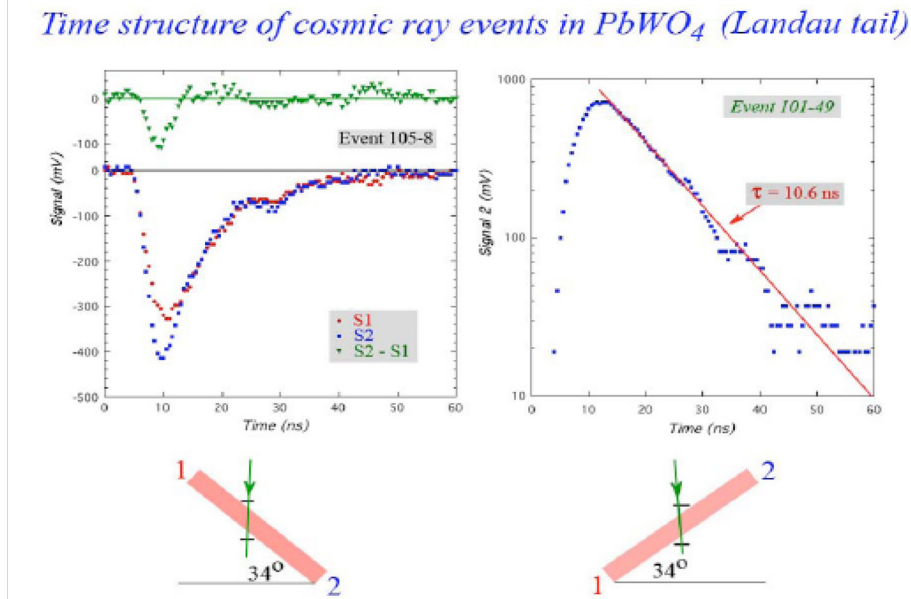


Figure 20 Decay time of scintillation light in PbWO_4 crystal and difference if scintillation and Cerenkov light (from [33])

1. of older fabrication crystal, with LY ~ 8

1.11 Crystal Strip Unit

The electronics of the PHOS calorimeter is fully embedded inside the cold and warm enclosures of 5 distinct PHOS modules of $56 \times 64 = 3584$ crystals each. Preamplifiers and APD diodes are attached to the PWO crystal ends with optical glue and operated in the cold volume at a temperature of -25 C. The signals of the CSP preamplifiers are connected to T-cards which collect all signals of one strip unit as depicted in Fig. 9. The grouped signals of one strip unit are connected via IDC flat cables to the FEE electronics which consists of digitization, control and trigger electronics (FEE and TRU).

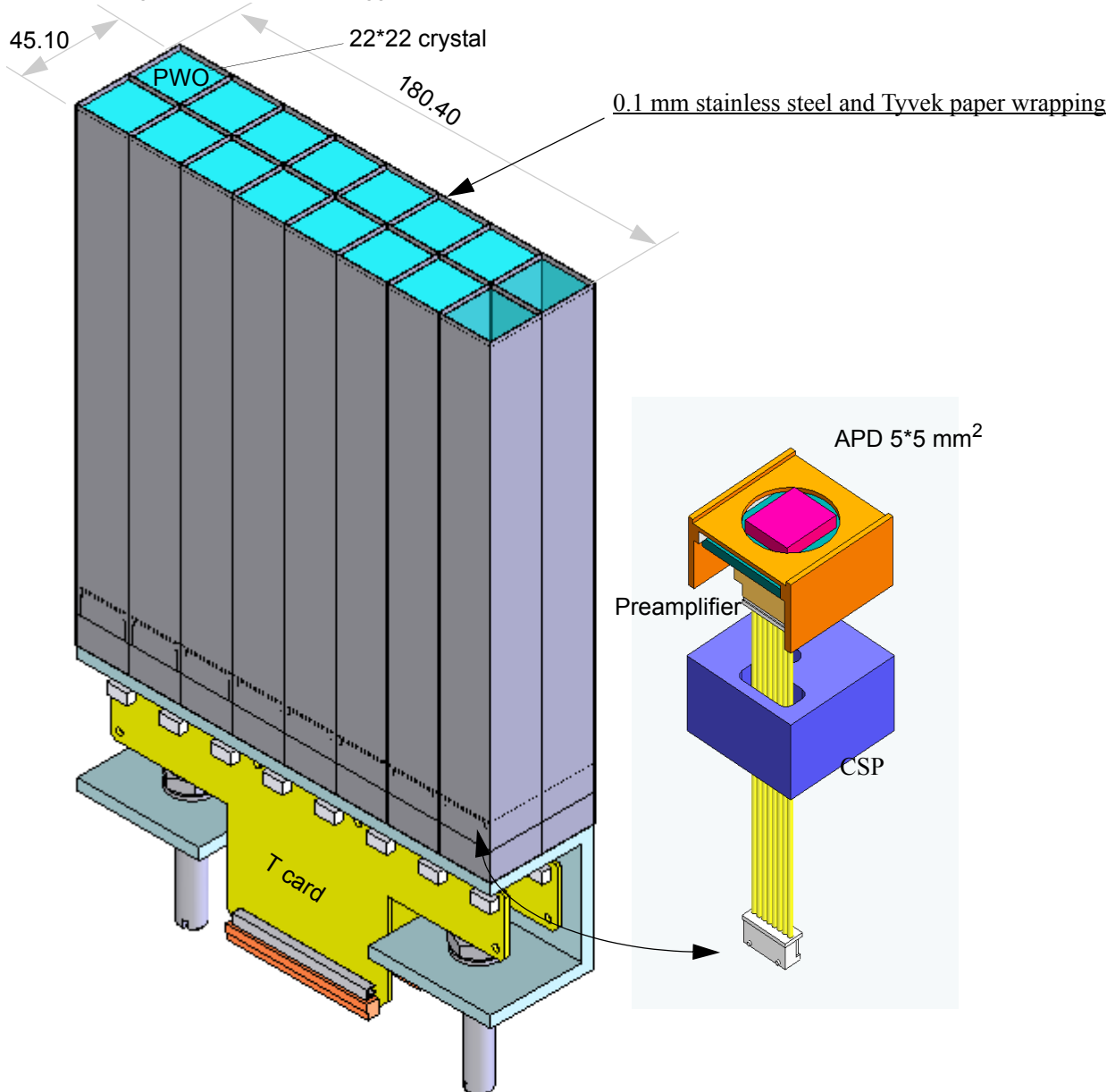


Figure 21 double strip unit consisting of 2×8 PWO crystals with APD/preamplifiers connected to two T-cards.
Note: A single 2×8 channel T-card is under design for new PHOS modules.

Figure 22 is the photo of a single PWO crystal on which the APD/CSP combination is mounted. The APD diode



Figure 22 Photo of a single PWO crystal mounted with APD/CSP

is glued to the crystal on one side and soldered to the CSP on the other side. A 6-conductor AMP cable provides both HV and LV connections to the CSP in addition to the analog signals for the FEE electronics.

The PWO crystals are mechanically mounted in units of 8 crystals called *single strip units*. These are connected to the FEE cards in parallel rows of *double strip units* like depicted in Figure 21. Due to this parallel arrangement, signal from 2*2 quadratic cells are available on a single FEE card, allowing to generate 2*2 analogue sums for the TRU trigger Unit.

Two double strip units in a column correspond to one FEE card for 32 crystals (2*16). Figure 23 is a photo of a single double crystal strip unit with T-card and mounting screws, connected via flat cable to the upper 16 channels of one FEE card.

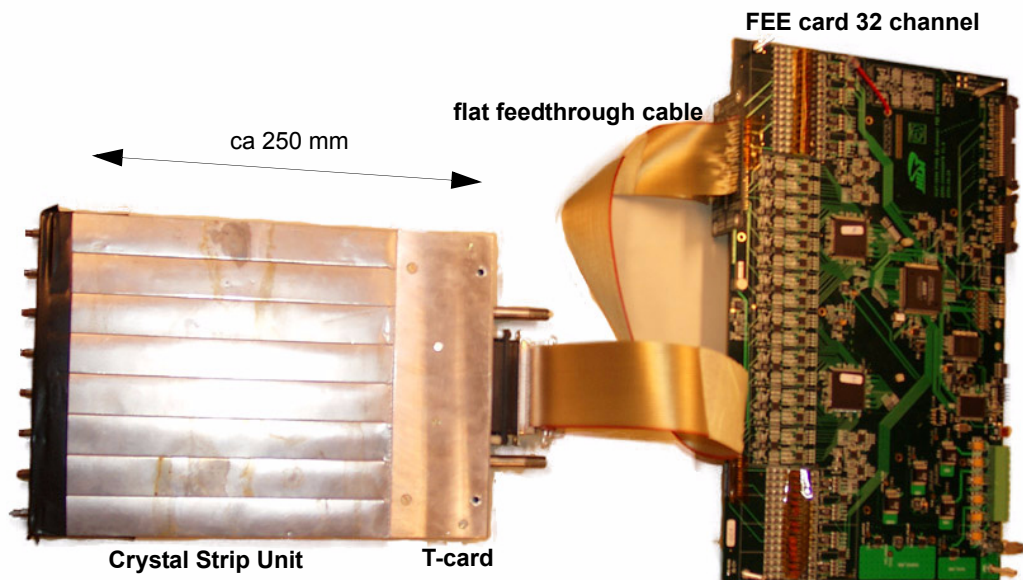


Figure 23 strip unit assembled with T-card and FEE card.

2 Avalanche Photo Diode (APD)

Avalanche Photo Diodes have a very high quantum efficiency up to 80% and a gain¹ $M = 10 \dots 100$ defined by the reverse bias voltage (order of 300-400 Volt). APD's consist of a reverse-biased p-n layer in which a high internal electric field provides avalanche multiplication of primary electrons. The p side is attached to another p++ doped layer for gamma conversion, covered by a very thin Si₃Ni₄ transparent window for passing the light.

Contrary to the initial choice of PIN diodes for PHOS [1], APDs were chosen, since PIN diodes are sensitive to the punch-through effect (nuclear counter due to dE/dx) for charged particles like muons, whilst this effect is much reduced for APD's [12] since their depletion layer (6 μm , compared to 280 μm for a pin diode) is much thinner.

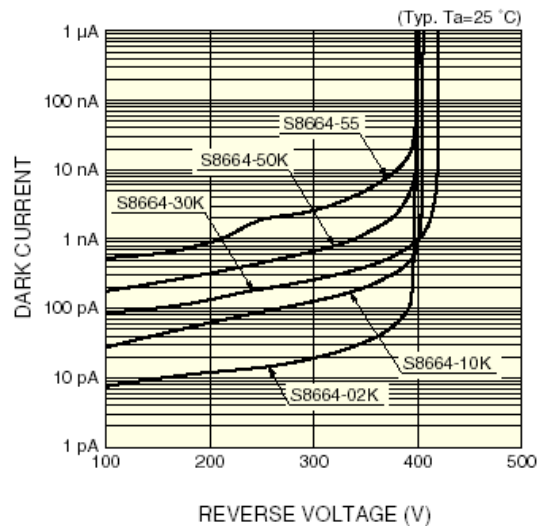
PHOS uses the same APD diodes which had been co-developed with Hamamatsu for the CMS experiment. Since PHOS operates at -25 C the CMS APD characteristics do not necessarily apply for PHOS.

The Hamamatsu S8664-55 (S8148) is a Si APD diode in ceramic package with sensitive area of 5*5 mm². The nominal gain $M = 50$ corresponds to a reverse bias Voltage of ca. 330-360 Volt @ -25 °C, with a terminal capacitance < 90 pF (see Figure 24). The dark current is an exponential function of temperature, hence the data sheet value of 4 nA at +25 C can be extrapolated to a value of order 1 ... 0.1 nA for -25 C.

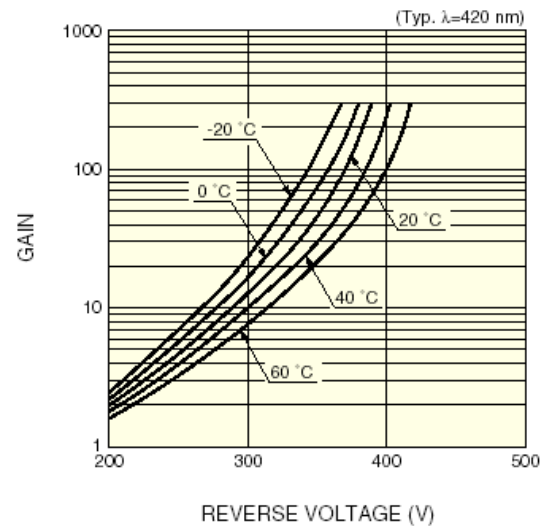
1. APD gains much beyond $M=100$ are in principle possible however relative APD gain stability and excess noise become too critical above $M=100$.

The typical characteristics of the Hamamatsu APD S8664-55 are shown in Figure 24

■ Dark current vs. reverse voltage



■ Gain vs. reverse voltage



■ Terminal capacitance vs. reverse voltage

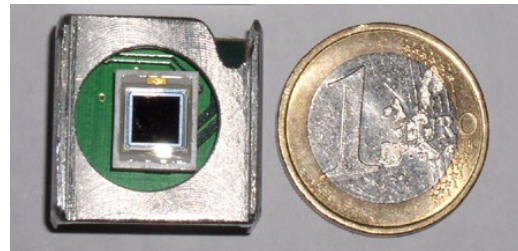
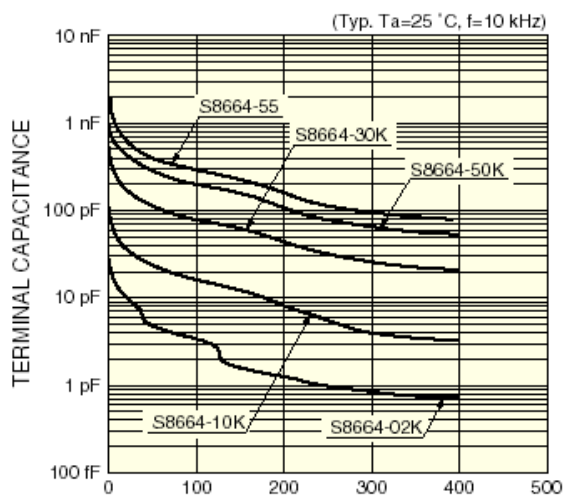


Figure 24 Hamamatsu APD S8664-55 with a sensitive area of $5 \times 5\text{ mm}^2$ shown on the back-side of the CSP with metallic mounting base fitting the size of a PWO crystal.

The bias voltage coefficient for constant gain $M=50$ as function of the reverse bias voltage is [39]

$$1/M \cdot dM/dV = +0.2\% / \text{Volt} \{M=50, -25^\circ\text{C}\}$$

2.1 APD gain settings

Considerable differences in individual APD gain exist for production batches when the same reverse-bias voltage at the PHOS operating temperature of -25 C is applied (Figure 25).

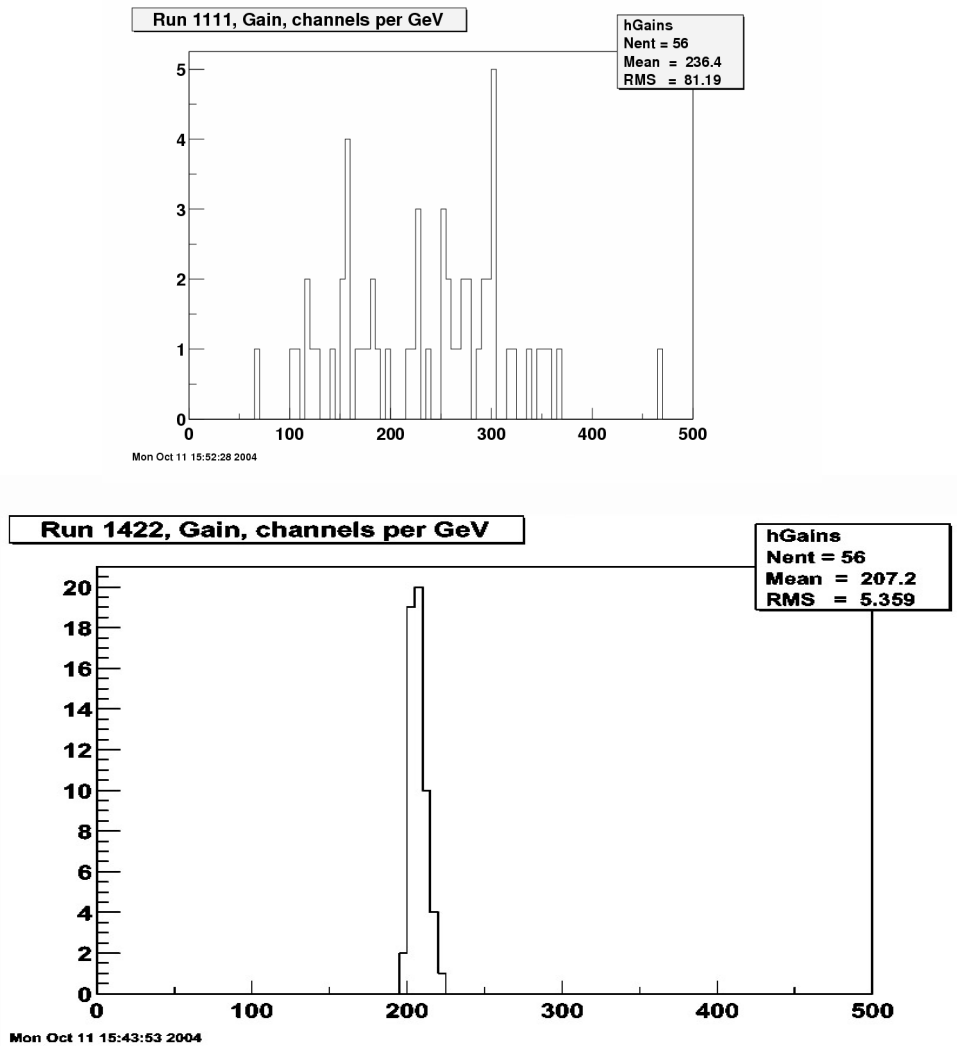


Figure 25 APD gain hardware calibration of 58 channels with 2 GeV electrons during 2004 testbeam. TOP: all APD same bias voltage: very large spread of relative gain. BOTTOM: calibrated to 5.3% via hardware APD bias control on FEE card

The individually programmable reverse bias voltage feature of the FEE cards allows that for *each* APD a programmable bias voltage range between 210...400 V is available. The Voltage settings are programmable via a 10 bit DAC under control of the PCM controller, which interprets DCS slow control commands.

The result of a first approximation calibration with the FEE-card-resident control logic is shown in the bottom of Figure 25. In this example a calibration level of only 5% was reached due to unavailability of fast online calibration tools during the 2004 october testbeam.

In the 2006 testbeam, a gain calibration level of 4 % was achieved (see Figure 26) by using the Hamamatsu APD gain database, extrapolated to -16 C . Further offline iterations achieve a level of 0.15% [30]

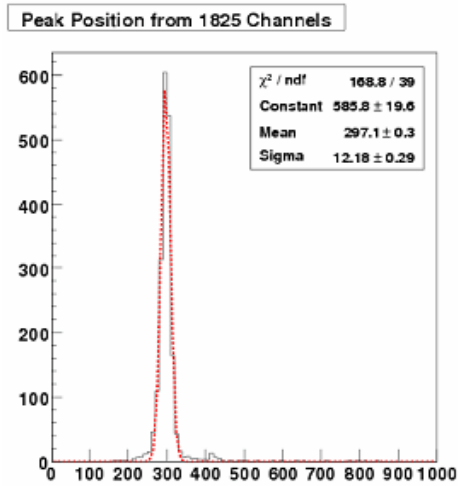


Figure 26 APD Gain calibration of 1825 channels during the 2006 test beam at -16 C. These APD settings which achieve a gain setting resolution of 4% were derived from the APD gain database provided by Hamamatsu for room temperature. The gains at -16 C were obtained by linear etrapolation.

2.1.1 APD gain at +20 C (Hamamatsu)

Hamamatsu S8148 APD's were delivered with a database¹ for individual bias Voltages for gain M=50 at room temperature. The distribution of gains as delivered in 2 batches is shown in Figure 27. The average bias

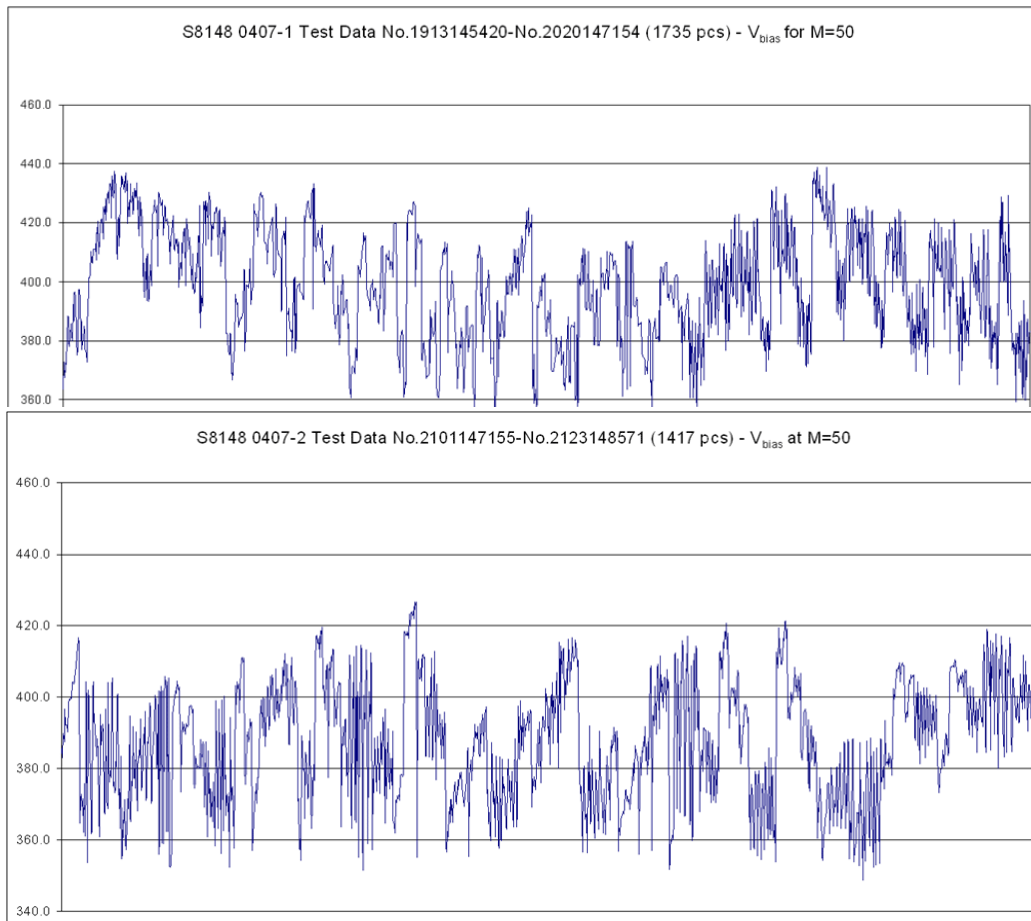


Figure 27 Bias Voltage for gain M=50 for two batches of APD deliveries of Hamamatsu in 2004.

voltages in batch A and B are significantly different. Also the M=50 bias voltages at room temperature of batch 1 lie significantly above 400 Volt and the spread in gain is significant. The bias voltages have to be reduced by 40 Volt when changing ambient temperature from +20C to -25 C

As compromise for gain dependency on voltage and temperature, the nominal gain chosen for the PHOS shaper on the FEE V1.1 corresponds to M=50. The individual APD gain is the only freely tuneable parameter to compensate for the fixed light yield differences of the crystals at constant temperature.

1. Excel sheet with reverse Voltages corresponding to Gain M=50 at room temperature

2.2 APD gain measurement/verification at +20 C

The Hamamatsu database for gain $M=50$ applies for +20 C. These gain figures were verified by using a constant light source (LED pulser with 470 nm wavelength) and measuring the peak amplitude $A(M)$ of the shaper pulse against the bias high voltage. The amplitude $A(M)$ for gain value $M=1$ is to be measured at the initial plateau of the photo-current at low bias voltges, typically at 20 Volt [NIM A 428 (1999) 413-431]. The horizontal line obtained by $A(M1) \times M$ crosses the gain curve above the bias voltage corresponding to gain M . Figure 28 shows the gain measurement for $M=50$ for two selected APD's with quite different characteristics APD # 2123148564 and APD #2201148644 at +20 C.

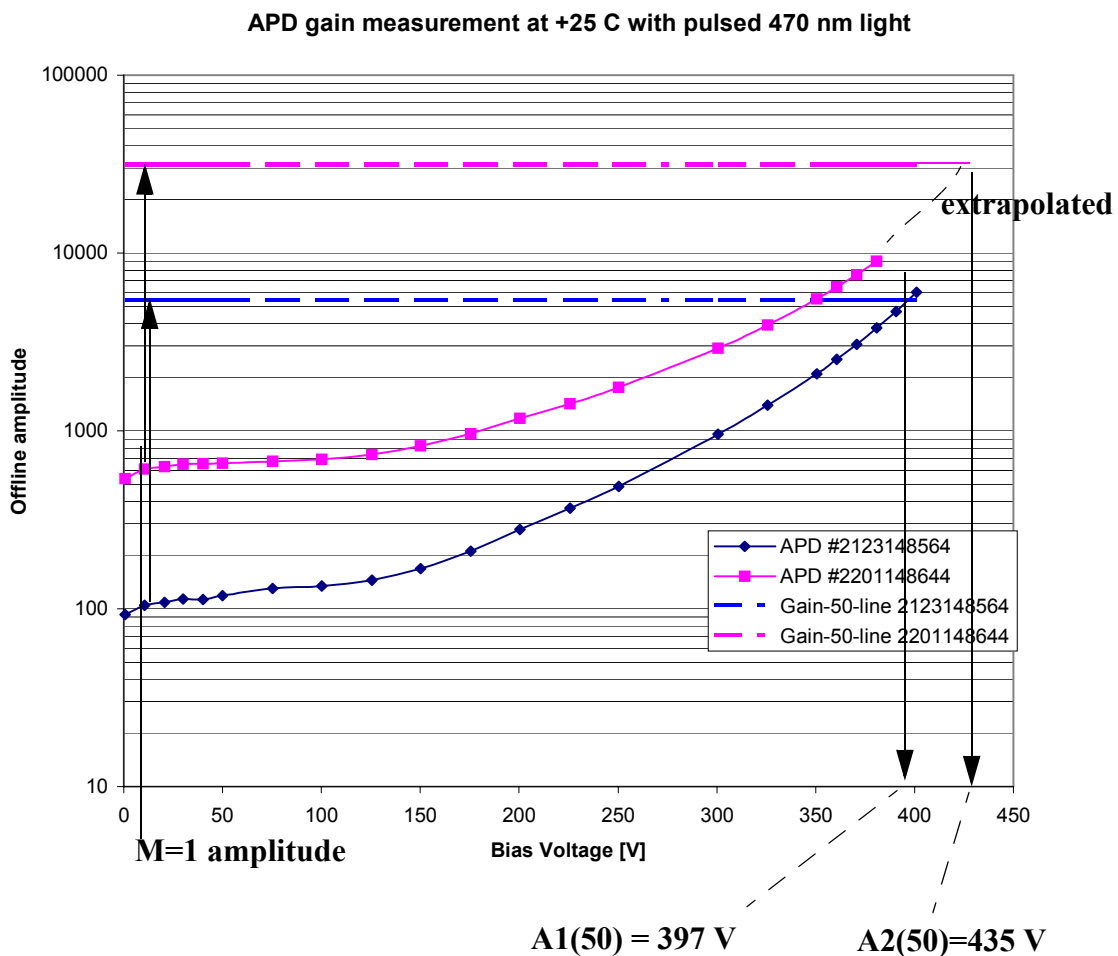


Figure 28 Confirmation of APD gain specified by Hamamatsu for 2 PHOS APDs at room temperature. The gain curve of the second ADP had to be extrapolated above 400 V since FEE card has a built-in Bias Voltage limit of 400V

The measurement confirms the Hamamatsu bias Voltages for $M=50$ at +20 C of 435 and 397 Volt respectively.

2.2.1 APD gain measurement at -25C (PHOS)

The same measurement as in Figure 28 were taken at -24 C, showing a shift in bias voltage (Figure 29) for a difference of 45 degree in temperature. The bias Voltages V_r for M=50 at -24C were measured as:

= $V_r(M=50)$ for APD # 2123148564 shifts from 397V to 354 V (**-43 V** from Hamamatsu value)

= $V_r(M=50)$ for APD #2201148644 shifts from 435V to 396 Volt (**-39V** from Hamamatsu value).

Since the gain M=50 is now below 400V for the APD sample #2201148644 which required 435 V at room

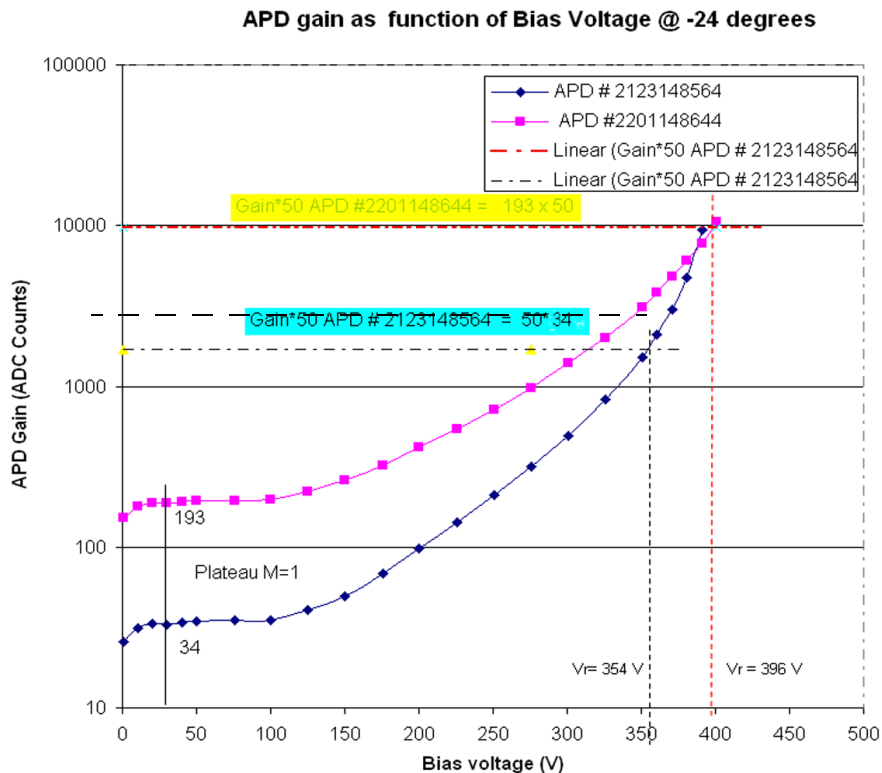


Figure 29 Gain measurement of the same APDs as in Figure 28 at -24 C operating temperature of PHOS.

temperature, the gain choice M=50 is confirmed for achieving the required APD gain over the whole Hamamatsu gain spread but at -25 C. The gain change for a temperature drop of 45 C corresponds to roughly 41 Volt over hence as a rule of thumb for PHOS:

$$dV/dT\{M=50\} \sim -0.91 \text{ V/C}$$

this corresponds to a temperature coefficient of

$$-1.1\% / ^\circ\text{C} \{M=50\}$$

2.2.2 APD gain choice for PHOS

A compromise between a high signal gain, noise and signal stability is required. With a practical APD gain range between 10 and 200, we have chosen a nominal gain value $M=50$ in combination with the FEE shaper gain. This choice has a 15 % lower excess noise than $M=100$ which has a direct effect on the stochastic term of the energy resolution. A low gain keeps the gain dependencies on temperature and voltage low (see Table 2).

The T and V dependencies have an important impact on the constant term of the energy resolution, in particular the constant (inter-calibration) term increases if the gain setting is too high: With a gain dependence of ~ 3.2 % per Volt at APD gain $M=50$ at room temperature, the bias logic can achieve with 0.2 Volt/bit an intercalibration precision of 0.6 %. Shown in Figure 30 is the percentual gain dependency on bias voltage as measured by CMS for room temperature: a factor 2 in APD gain increases the dependency by a factor 2. i.e if the gain would be chosen as $M=100$, the gain dependence would be 6.6 per Volt hence the APD intercalibration precision would be 1.3 % per set bit.. The major APD characteristics for PHOS are summarized in Table 2.

Table 2 APD parameters S-8664-55

M=50 parameters	Value @ +20C	PHOS Value @ -25 C
active area	25 mm ²	
terminal capacitance (Figure 24)	90 pF	100 pF, 10 pF for FET input added
Dark current (Figure 24)	3 nA	estimated 1 nA
Quantum Efficiency (Figure 17)	70 %	M=1 and 420 nm
CMS measured gain dependence on bias voltage $1/M \cdot dM/dV$ (M=50)	3.3 % per Volt @ room temperature for M=50 (??)	PHOS: 0.2 % per Volt for -25 C
CME measured gain dependence on Temperature $1/M \cdot dM/dT$ (M=50)	-2.2 % per degree	PHOS: -1.1% per degree

3 Charge Sensitive Preamplifier (CSP)

The charge sensitive preamplifier CSP [29] produces an output voltage step which is proportional to the charge produced by the APD on its input capacitance C_D . The charge Q_{APD} is measured over C_f due to the high gain A of the amplifier since the input of the amplifier is virtually at ground potential, therefore the Voltage at the output of the amplifier (without R_f) is

$$V_{out} = \frac{Q_{APD}}{C_f}$$

In order to discharge C_f for the next event (1 kHz maximum channel rate assumed), a discharge resistor R_f is connected in parallel with C_f and dimensioned to discharge the capacitor with a time constant of 0.1ms. This auto-discharge method has as a side-effect a small baseline movement which needs to be compensated by the pole-zero-suppression on the FEE card.

The maximum CSP preamplifier signal of the PHOS dynamic range (80 GeV) corresponds to 2.34 Volt, though the CSP step output may range beyond 5 Volt in order to allow for signal pileup at the CSP level (removed by the shaper). The CSP capacitor C_f is automatically discharged via the resistor R_f with a time constant of ca. 100 us. This limits the single channel input signal rate to less than 10 kHz.

Figure 30 shows the principle of the CSP used by PHOS.

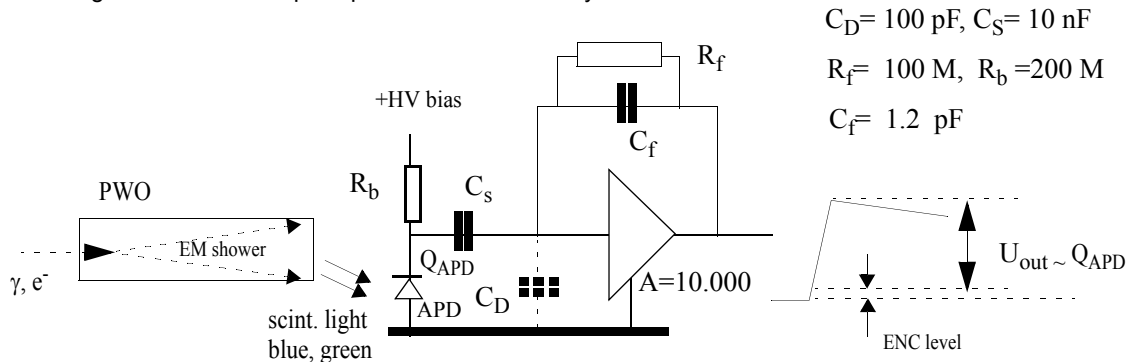


Figure 30 Charge Sensitive Preamplifier (CSP) principle

The input charge Q_{APD} is a linear function of the crystal light yield and given by the number of electrons generated by the APD including gain amplification. The electrons are multiplied by the APD amplification gain M since the APD diode is reverse biased up to +400V via a very high resistance R_b . The high voltage is DC-wise separated via C_s from the input of the pre-amplifier.

The Photo Figure 31 depicts the component and connectors side of the CSP. The APD is mounted on the back-side. The test capacitor C_5 serves for injecting charge directly to the input allowing to test the CSP pulse response. This capacitor must not be mounted in the PHOS since it is also a potential source of pickup noise via the pin 6 connection and cable of the molex connector.

The CSP preamplifier dissipates ca. 60 mWatt, hence the total heat dissipation of all 3584 CSP's inside the cold volume of a PHOS module amounts to 215 Watt. A closeup photo shows the connector side of the CSP (Figure 31).

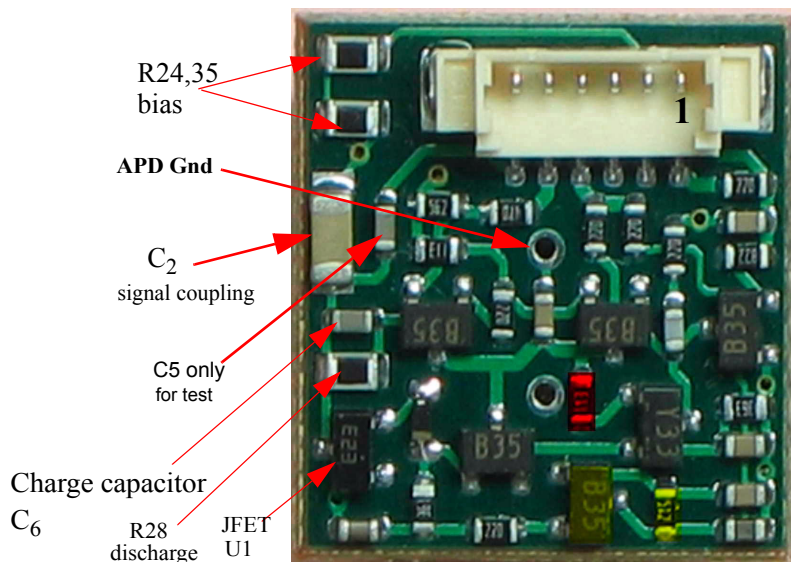


Figure 31 CSP PHOTO

Photo of CSP 19 x 19 mm² preamplifier with 6 pin Molex connector. The test capacitor C5 is only to be mounted for testing.

Pinout Molex 53047

- 1.....-6 V, 2.2 mA
- 2.....HV Bias
- 3.....Gnd
- 4.....+12 V, 4.2 mA
- 5.....CSP-Out
- 6.....(Test in)

The schematics of the PHOS CSP is shown in Figure 32. It is alimented by +12V (4.2 mA) and -6V(2.2 mA) and uses a low noise J-FET transistor of very high gain as amplifier.

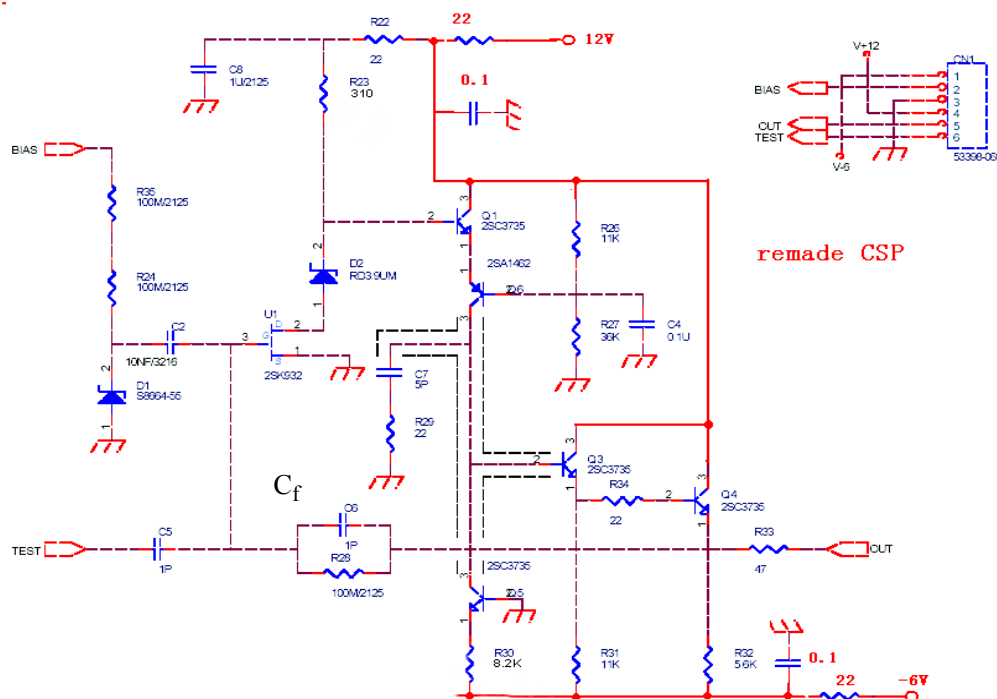


Figure 32 Schematics of PHOS preamplifier CSP

The CSP input stage is a J-FET transistor (2SK932) with forward admittance g_m as depicted in Figure 33 . For

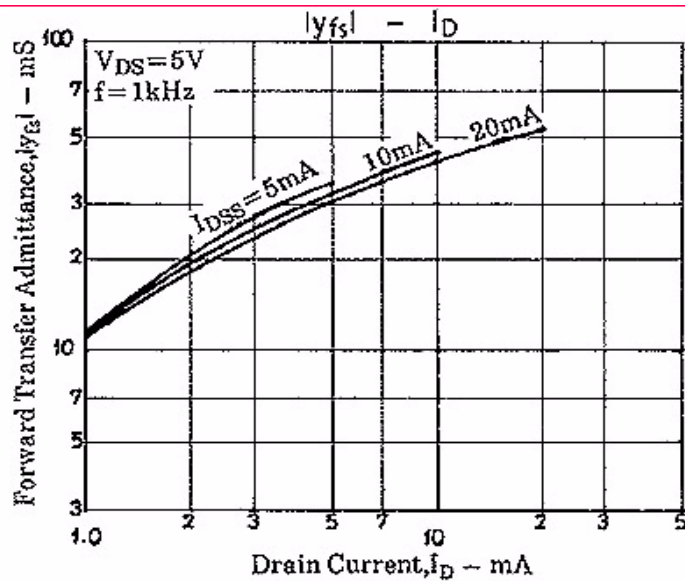


Figure 33 Forward admittance (g_m) of the 2SK932 input stage J-FET.

the noise calculation, the serial noise (voltage noise) is produced by the Johnson noise in the input of the J-FET Transistor can be described by a series resistor R_s whose resistance is inversely proportional to the input forward transconductance g_m . For modern J-FET transistors the proportional constant is a ~ 1 . For a JFET drain current of 4 mA the forward admittance is ca 30 mS With this:

$$R_s = \frac{a}{g_m} \approx \frac{1}{g_m} = 33\Omega$$

The input capacitance of the CSP consist of 2 parts:

$$C_D = C_{APD} + C_{FET} = 100\text{pF}$$

The APD has ca. 90 pF terminal capacitance at 350V, the input capacitance of the 2SK932 J-Fet is 10 pf.

The original Kurchatov/Bergen design [14] of the CSP preamplifier was tuned for amplitude independent rise-time as shown in Figure 34 for a 4 ns test input pulse. A small overshoot of the output pulse is present.

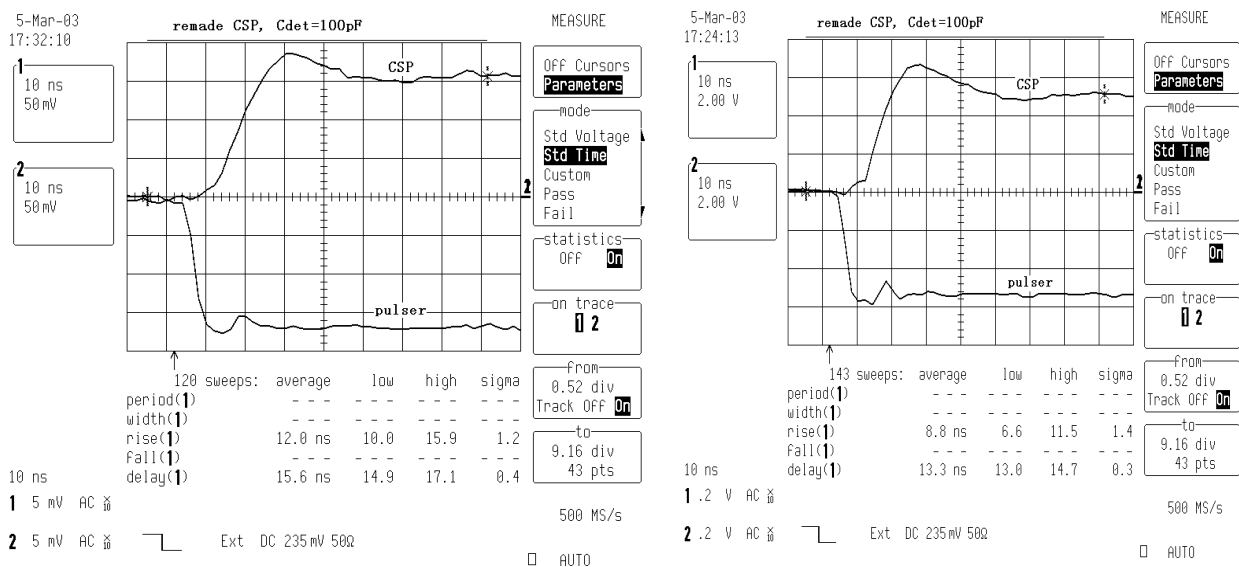


Figure 34 Tuned CSP for risetime 9...13 ns over dynamic range (max 5 Volt) with 4 ns input signal (from [14])

Figure 35 shows a CSP mounted together with a PWO crystal. The APD, soldered to the CSP backside, is

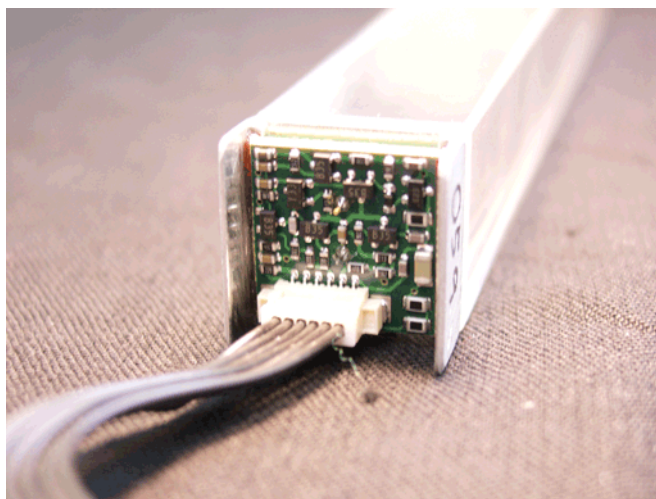


Figure 35 Preamplifier and APD attached to PWO crystal

glued to the crystal.

The parameters of the Bergen/Kurchatov CSP, tuned for equal risetime (9.. 13 ns) over the full dynamic range are:

sensitivity = 0.833V/pC or 0.133 uV / e-

open loop gain A=10000

feedback capacitor effective $C_f=1.2$ pF (= 1pF plus parasitic)

Output Voltage for APD gain M=50: 26.7 uV per MeV + 69 uV(ENC) (see Figure 18)

- rise time 15 - 20 ns over full range (see Figure 34)
- discharge time constant: nominally 100 us via 100 MOhm resistor
-
- "DC output level = -0.5V
- Full swing over energy range: 2.4 Volt for CW shaper
- "power = 12 V (4.2mA), -6V (2.2mA)
- "power dissipation = 64 mW
- power dissipation of all CSP's in 1 Module = 230 Watt

3.1 Noise at the CSP output

The CSP produces a step voltage function which has a very rich fourier spectrum. The electronic noise charge ENC at the level of the CSP is [14]

$$ENC = 200 e + 3.2 e / pF * C_{in}(pF)$$

The Detector capacitance of APD and JFET input capacitance add up to $C_{in} = 100$ pf, such that the equivalent noise charge at the output of the CSP (not taking into account pickup noise by the cable between CSP and FEE cards) is

$$ENC_{CSP} = 520 \text{ electrons}$$

The subsequent shaper (see chapter 5) removes unnecessary parts from the step function fourier spectrum and reduces such the noise further by about 50%.

The noise dependency at the CSP is a linear function of the detector capacitance. As will be seen later the noise dependency after the shaper is a quadratic function of the detector capacitance.

As shown in Figure 24 the APD capacitance reaches very high values when no reverse bias voltage is applied. In these situations, the noise is magnified by a large factor. This situation can however be very useful for occupancy plots as discussed in 4.5 .

3.2 Simple CSP test with PWO and cosmic particles

Figure 36 shows an oscilloscope measurement of the CSP output Voltage step with an APD at room temperature, and the PWO crystal traversed by a cosmic Muon¹. With 1m of flat cable to the FEE input, the risetime to a step voltage level of ca 7.6 mV (trace 3 and B) is ca. 40 ns and includes a small overshoot. The signal risetime includes the scintillation light decay time of (an old) PWO crystal which was used for this purpose.

1. The PWO crystal was positioned vertically in absolute dark and the APD operated with high gain (M~100) The oscilloscope was triggered by the shaper output. Cosmic events along the whole crystal occur only very rarely (ca 8 per hour) and deposit ca 170 MeV. The event shown here is an event which traversed the crystal under some angle since its signal amplitude is less than the rare vertical events.

The FEE shaper produces from the CSP step output a pole-zero-compensated Gamma-2 like output pulse of 2 μ s peaking time and 2x 25 mV peak amplitude at the ADC.

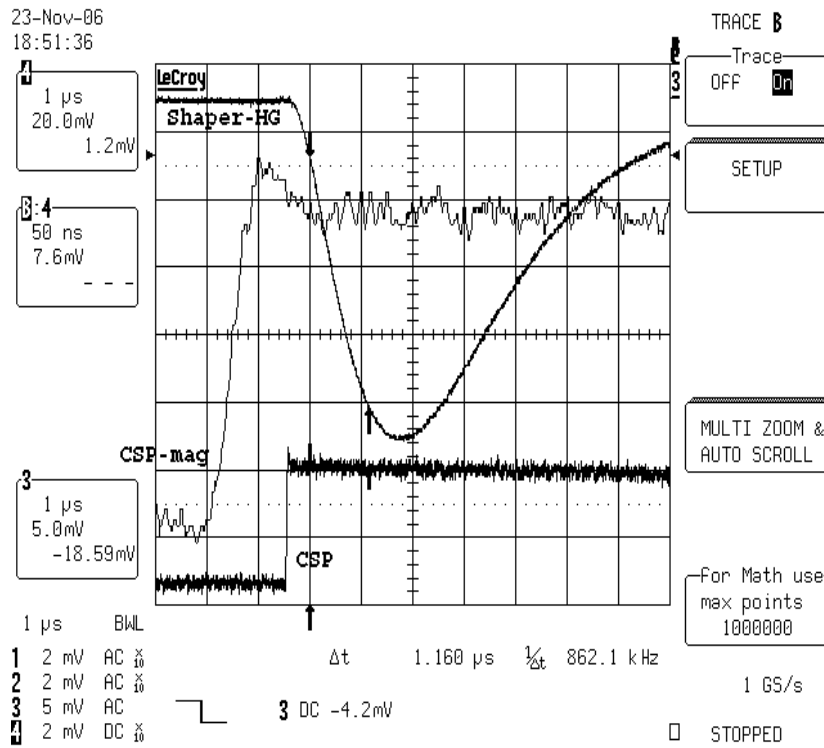


Figure 36 Oscilloscope measurement of the CSP output of a cosmic muon event in the PWO

trace 4= step Voltage (CSP)

trace B: CSP magnified

trace 3: shaper response

4 Electronic Noise

With the aim to achieve a good energy resolution also at low energies (compare 1.3), the FEE shaper was designed with a low-noise input buffer stage.

A low noise level is important for achieving good Energy resolution at low Energies in particular for calibration with muons (~ 176 MeV, see 6.2), and for adequate resolution of the two-photon invariant mass peaks of the π^0 (134.97 MeV) and η (547.75 MeV) for yield measurements and for energy calibration of the calorimeter.

The noise of cascaded amplifiers (depicted in Figure 6) with N1 and N2 noise levels is calculated as

$$N_{\text{noise}} = \sqrt{N1^2 + \left(\frac{N2}{K1}\right)^2}$$

K1 is the amplification of the first buffer stage. By choosing $K1 > 1$ the contribution of the shaper noise N2 can be reduced by choosing a buffer with a low-noise figure N1. In the FEE shaper $K=2$.

The standard noise analysis [38] is depicted in Figure 37 below. It dissociates the noise sources in

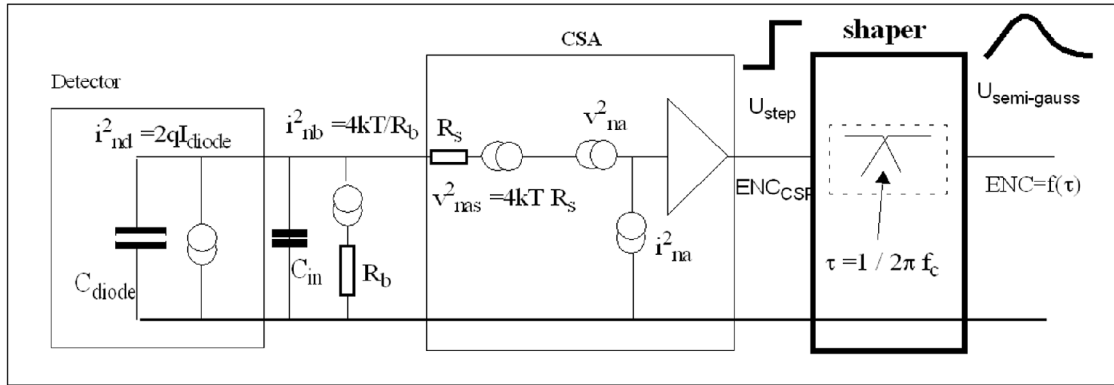


Figure 37 Equivalent noise sources: parallel current noise and serial voltage noise.

voltage and current noise with their generators (temperature, leakage currents etc.). The equivalent noise ENC_{CSP} from the CSP step function is passed through the shaper bandpass which retains the main signal components and suppresses the noise components towards low and high frequencies. The shaping time constant f_c determines which center Fourier components of the signal are passed. The shaping time constant t can be chosen such that the noise after the shaper is minimal. The shaping time relates with the center frequency f_c of the shaper bandpass via $\tau = 1/(2\pi f_c)$.

The noise components are:

- Current noise (parallel): With the Boltzman constant k and absolute temperature T , the mean shottky current through the reverse-biased detector APD diode is $2q I_{\text{diode}}$. This current is defacto equal to the thermal current $4kT/R_b$ generated by the bias Resistor R_b which is effectively a parallel shunt to the detector capacitance C_D . Due to the current equivalence, the shunt resistance can be described as $R_b = 4kT/2q I_{\text{diode}}$, i.e. with a 200 pA reverse current at -25C ($T=250K$) the 200 MOHM bias resistor is reproduced.
- Voltage noise (serial) $4kTR_s$ thermal Johnson noise at the amplifier input given by the seial Resistor in the input if the JFET Transistor, R_s
- the overall present $1/f$ noise

The Equivalent Noise Charge (ENC) at the output of the shaper is a function of the shaping time constant τ at the absolute temperature T . The ENC noise parametrization depends on parallel, serial, and constant noise sources, and of the detector capacitance.

- the current noise is proportional to the shaping time τ
- the voltage noise is inversely proportional to τ
- the $1/f$ noise is independent of τ

With an estimate for the $R_s = 2/3 * (1/g_m)$ where g_m is the forward transconductance of the JFET transistor of the CSP, the ENC noise after the shaper as function of shaping time is given by:

$$ENC^2 = \frac{4kT}{q^2 \cdot R_b} \cdot F_p \cdot \tau + \frac{4kT}{q^2} \cdot \frac{2}{3} \cdot \frac{1}{g_m} \cdot F_s \cdot \frac{C_d^2}{\tau} + C_d^2 \cdot \text{const}$$

For the PHOS electronics the following values apply: $g_m = 30 \text{ mS}$ (see chapter 3), $C_d = 100 \text{ pF}$ (APD= 90pF @ -25 C, JFET=10 pF). The noise figures [36] for a CR-RC2 shaper are: $F_s = 0.84$ and $F_p = 0.63$.

Figure 38 shows the relative ENC dependence on the shaper time constant τ under neglection of the constant 3rd ($1/f$ noise)

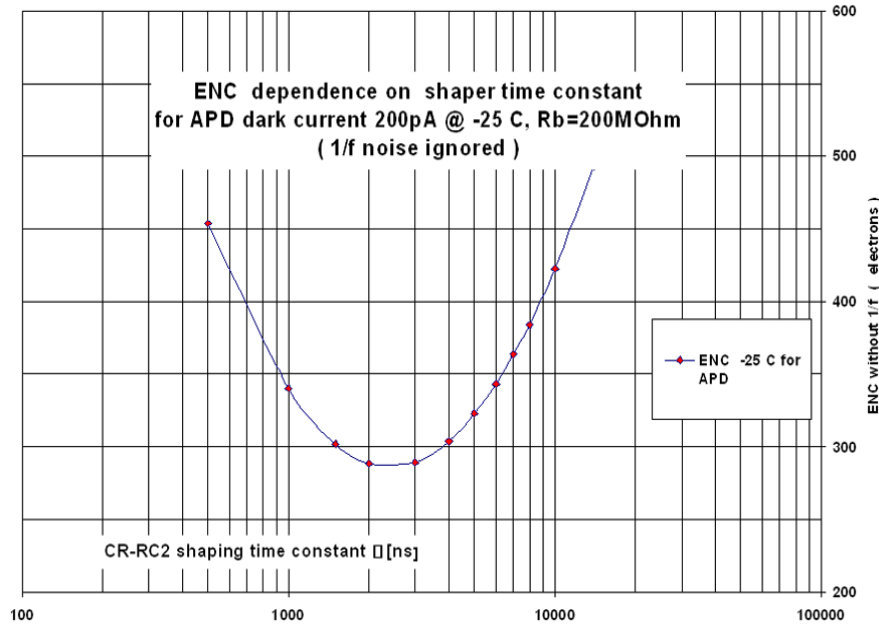


Figure 38 ENC noise after FEE shaper as function of shaping time constant for ambient temperature of -25C. The optimal shaping time would be 2us,

Though the minimum ENC lies at ~ 2 us, a compromise of 1 us was chosen for PHOS in order to enhance offline timing resolution (due to the higher Fourier spectrum at less shaping time.

4.1 Electron - CSP voltage equivalence

With a charge capacitor of 1.2pF the CSP voltage/charge conversion gain $V = Q/C$ is:

$$0.833V / pC \text{ or } 0.133 uV / \text{electron}$$

With the definition that 1 ADC count is set to 5 MeV for the high gain it follows (with 1 Altro ADC count = $1V/1024 = 0.9765$ mV and with shaper gain = 6.5)

$$5 \text{ MeV} = 976uV / 0.133 uV * 1/6.5 = 1129 \text{ electrons}$$

$$1 \text{ MeV} = 225.8 \text{ electrons}$$

$$1 \text{ ADC count} = 1129 \text{ electrons}$$

Further:

$$1 \text{ MeV} = 195.2 uV \text{ (at the ADC)}$$

$$1 \text{ MeV} = 30 uV \text{ (at the CSP output)}$$

4.2 Noise measurement as function of the APD gain

Figure 39 shows the single channel RMS noise, measured offline as function of the APD gain (bias voltage)

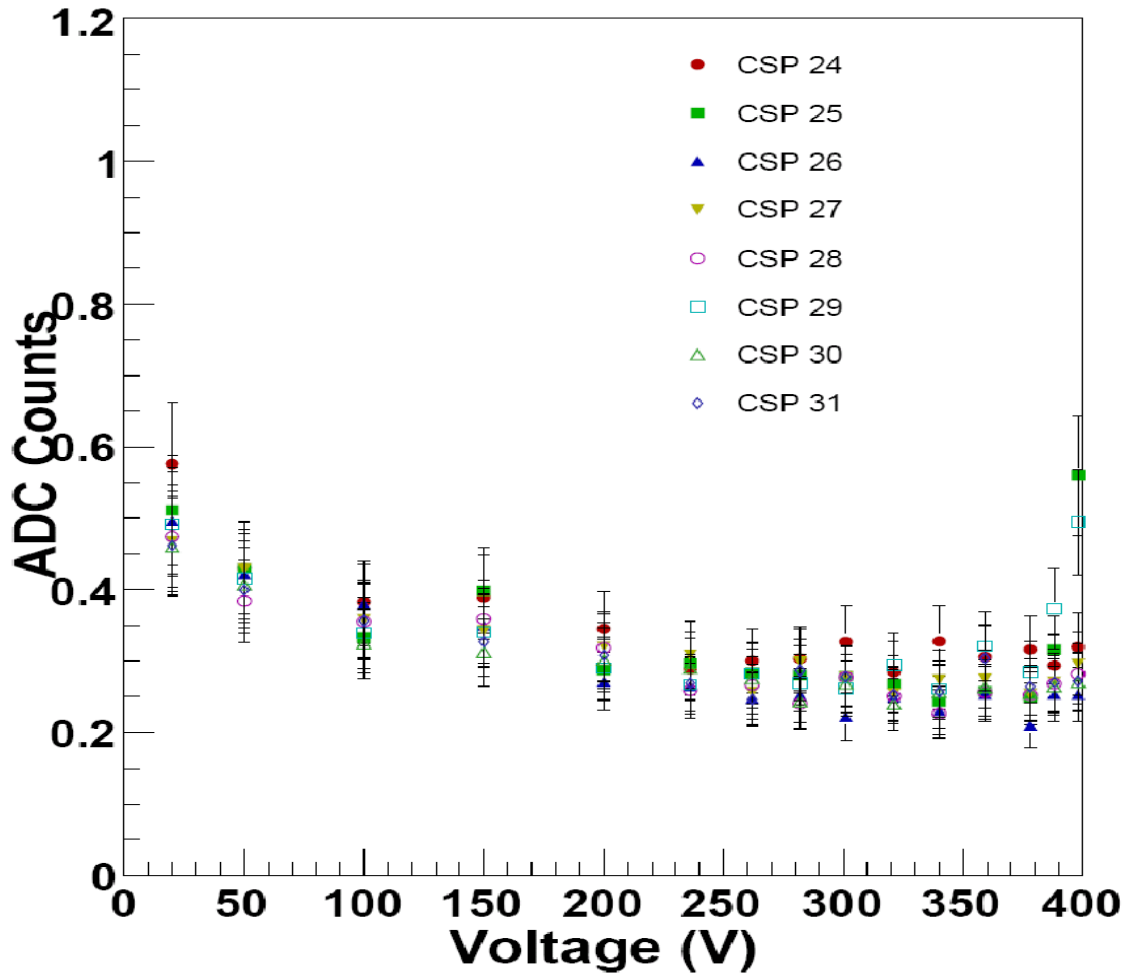


Figure 39 Noise measurement as a function of the APD bias Voltage for 8 APD's.

over the full range at -25 C. By comparing 8 APDs, the minimum lies at ca 300-360 Volt, corresponding to a gain $\sim M=50$.

With the equivalence of 1 ADC count = 5 MeV, this measurements results in an average single channel noise for APD gain $M=50$ and -25 C:

- 0.3 ADC counts
- 1.5 MeV
- 339 electrons

See 4.1 and note the correspondence with the calculated noise in Figure 38 for 1 μ s shaping time.

The corresponding 3x3 noise is 4.5 MeV¹.

4.3 Offline Pedestal and Noise measurement

The RMS noise is measured offline from the pedestal noise over the N measurements. N is normally the number

$$\text{RMS}(N) = \sqrt{\frac{1}{N} \sum_i (y_i - \text{Mean})^2}$$

of pre-samples before the signal, hence a number smaller than 10.

The ROOT Macro **get_pedestalAll.C** calculates the RMS noise and pedestal for all high or low gain channels in a FEE card.

In the ROOT environment this macro is called as

.x get_pedestalAll.C(RunNumber, highOrLow)

where *RunNumber* is the run number and *highOrLow* takes value 1 for high gain channels and 0 for low gain channels.

Root generates individual event histograms from which the mean and RMS is taken as event pedestal and event RMS noise. Then these event-pedestals and event-RMS values are sorted in two new histograms of all events, resulting in the pedestal and RMS noise, together with their errors. Figure 40 shows such pedestal and RMS noise measurements which were taken with PHOS FEE cards and APD/CSP temperature of -25C in a refrigerator. For this measurement, only the presample area of the shaper pulses like shown in Figure 42 were used, which allows to separate events with crosstalk or pileup noise.

1. The 3x3 noise measured during the 2006 testbeam is a factor 2-3 larger, due to several factors: 1.) not reaching the PHOS operating temperature, namely -16 C instead of -25 C, which means 30% less lightyield 2.) by using pedestal runs which include crosstalk and pileup.

The RMS noise taken from “pedestal runs” is usually higher since it includes all other noise sources and does not allow to separate noisy events. The measurement of Figure 40 is therefore a purified RMS noise measurement showing the intrinsic RMS noise after the FEE shapers for the PHOS operating environment, as 1.1 MeV or 250 electrons.

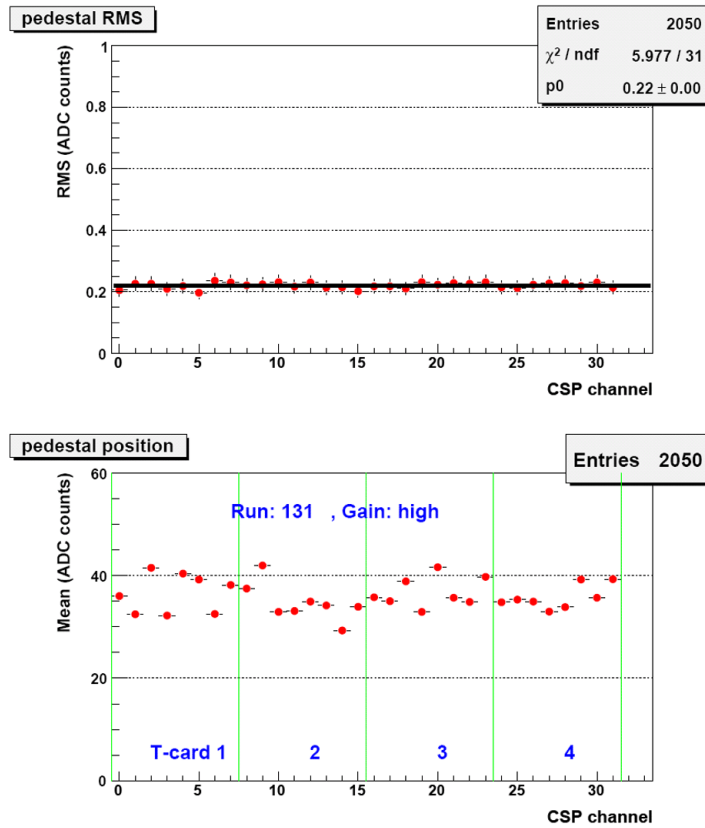


Figure 40 Output of Root macro `get_pedestalAll.C()` for 1 FEE card. The upper plot depicts the RMS noise from pre-samples of all 32 high gain FEE channels in ADC counts. The lower plot shows FEE pedestals in ADC counts. 1 ADC count corresponds to 5 MeV or 1130 electrons. The noise level of 0.22 ADC counts corresponds to 1.1 MeV or 250 electrons. The average pedestals for high gain channels lie around 35 ADC counts

The noise level obtained by this measurement is with 1.1 MeV better than the two previous methods.

Note: The pedestals of each channel are automatically measured by the Altro VPED register (See 11.1.2 ,) i.e. should result in the same value as the offline measurement

4.4 Noise measurement summary

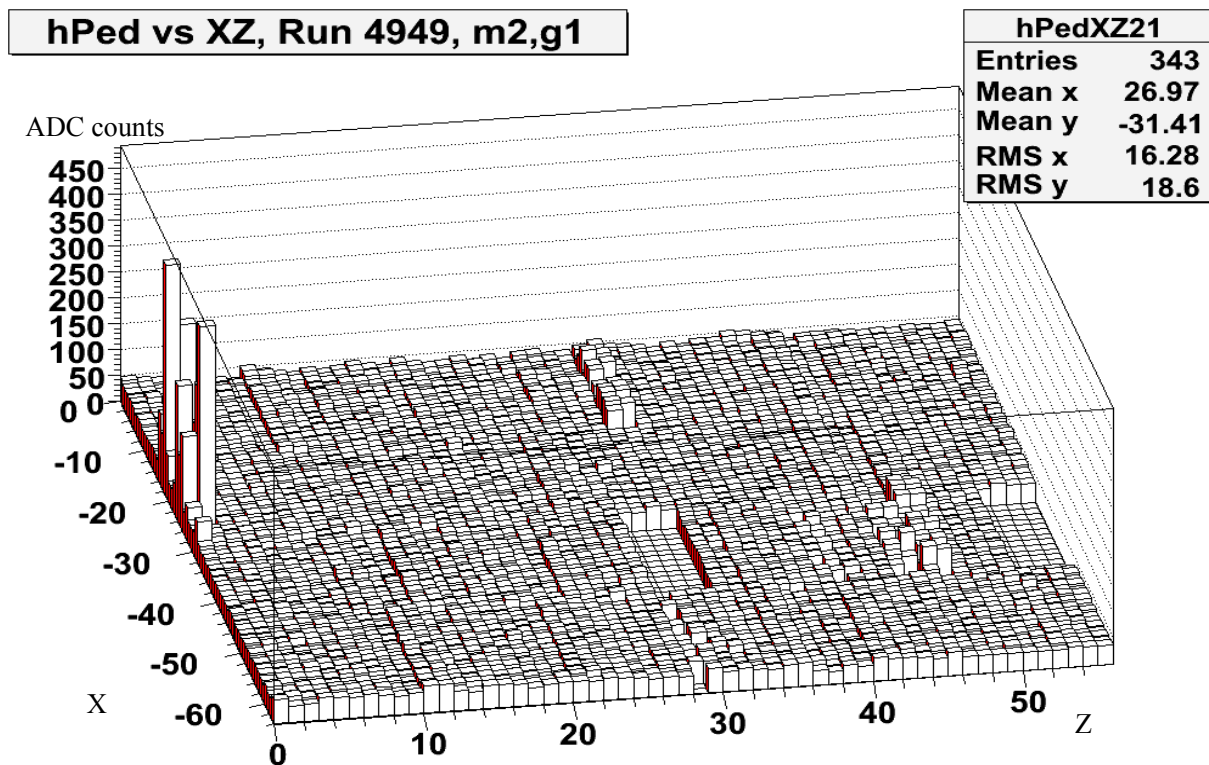
In summary the noise level of PHOS FEE electronics is:

- Calculated (Figure 38) = 340 electrons = 1.5 MeV
- Measured with APD(Figure 39) = 339 electrons = 1.5 MeV
- Direct offline measurement (Figure 40) 250 electrons = 1.1 MeV

4.5 Artificial noise plots

The detector capacitance increases from ~ 90 pF under normal reverse bias operation at $M=50$ to several nF when no reverse bias voltage is applied. Since the ENC noise increases quadratically with the detector capacitance, significant noise levels appear when the APD reverse bias voltage is not applied. This feature is however useful for testing the alive status of the detector channels with “artificial noise” (Figure 41)

The artificial noise plot of a complete PHOS module (APD bias=0) in the x-z plane shows order of 50 ADC count noise when no reverse APD bias voltage is applied.



Thu Nov 16 13:24:44 2006

Figure 41 Noise plot of PHOS module with reverse bias Voltage = 0. The average noise under this special condition extends up to 50 ADC counts. *Note: the channel noise with reverse bias Voltage is an order of magnitude less < 1 ADC count (see Figure 39)*

The noise plot of Figure 41 exemplifies the usefulness of the artificial noise method which also excludes all problems due to wrong APD bias voltage: Some noiseless or over-noised zones are clearly identified in this plot (measured at room temperature). There appears to be a leak of light at the left side edge ($z=0$) and at $z=30$ and $z=54$ contiguous areas (T-card connectors) are missing. This can be due to either a hardware problem (no connection) or a readout problem (area is not properly initialized for readout)

Figure 42 depicts a noise plot of one quarter (896 crystals) of a PHOS module. There are no major problems apart that slight steps in pedestal levels along the FEE boundaries (along x) are visible. There are also 2 single channels with pedestals significantly above the average of the other 896 channels (0.2 %)

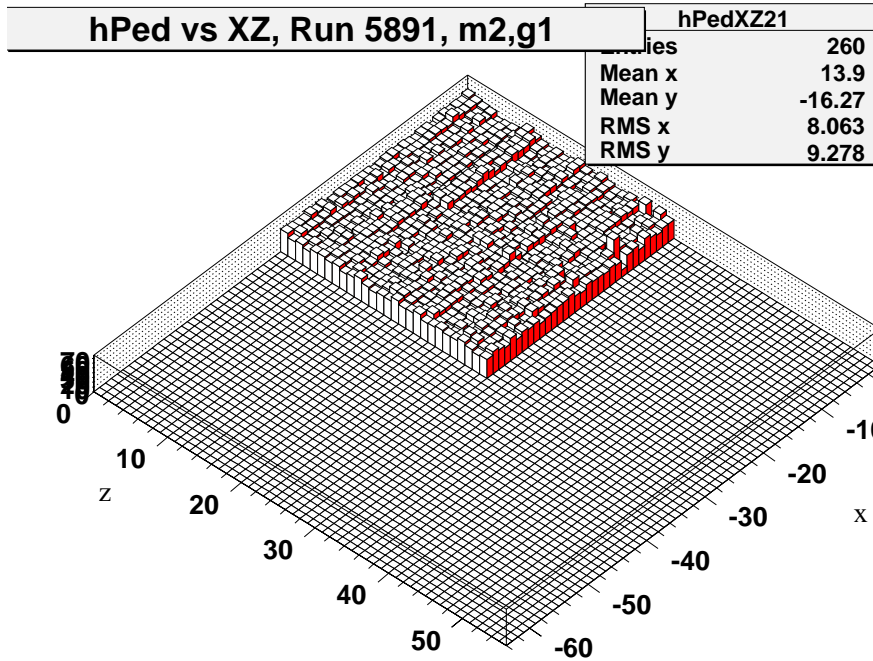


Figure 42 Noise plot of one readout partition (two RCU branches). The pedestals are averaging to ca. 40 ADC counts.

4.6 PHOS channel map (1st module)

The channel map of the first PHOS module (64 x 54 crystals)is shown in Figure 43

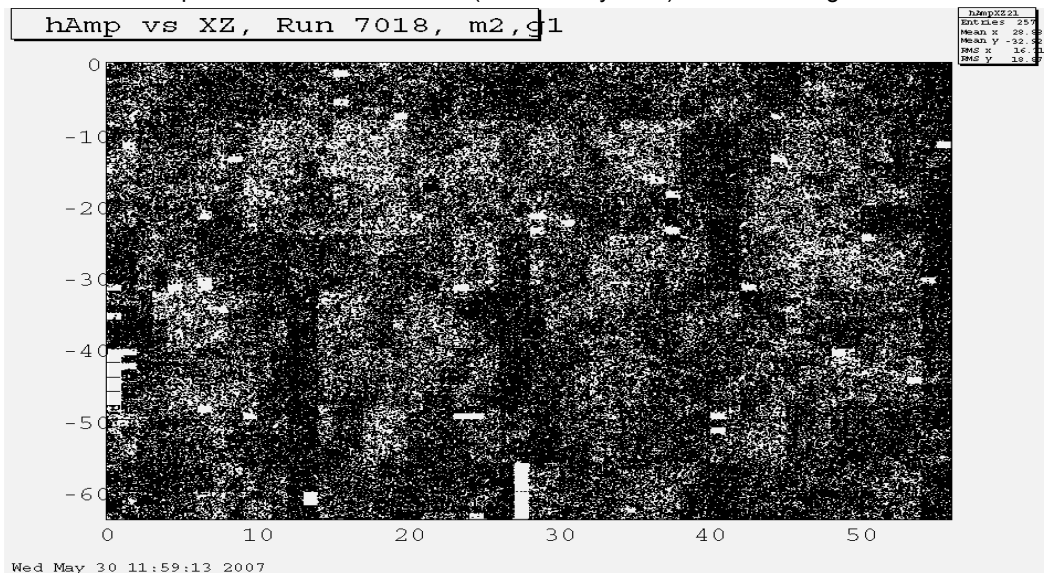


Figure 43 Occupancy / dead channel map of the first PHOS module

5 PHOS shaper

The shaper is a filter which separates the signal from noise without loss of information. The input signal is the Voltage step from the Charge Sensitive Preamplifier the output is a semi-gaussian pulse. The Voltage step is proportional to the charge generated by the APD, as well as is the peak of the semi-gaussian. In practise, the shaper is a bandpass for the voltage step signal (like Figure 36) which is composed of a very large Fourier frequency spectrum. The shaper bandpass suppresses low and high frequency components in order to retain only information of the step height and to cut all noise contributions from the low and the high frequency spectrum, produced by the APD, CSP and other.

Typically shapers consists of a 1st order high-pass (differentiator) and n^{th} order low-pass (integrator) of the same time constant $\tau=1/(2\pi f_c)$, where f_c is the center frequency of the bandpass. The order of the shaper defines the power attenuation slope above f_c . An order n shaper has a slope of n^* (-20db) per 10x frequency. The order of the shaper is a tradeoff of noise suppression and cost.

The total ENC noise for first order shapers is generally 12.5 % higher than for second order shapers. For the PHOS FEE electronics, the best compromise for an implementation of the shaper in discrete logic was $n=2$ (second order). The implementation of the PHOS shaper in discrete logic has the advantage of being "user configurable". The shaping time and the shaper gain can be chosen by a set of resistors and capacitors which depend on the detector requirement. A first example of a different shaper implementation is EMCal with a shaping time a factor ten less than PHOS.

Figure 44 shows the characteristics of the PHOS shaper as combination of a 1st order differentiator (small blue dotted, rising slope) and of a second order integrator (full red line, falling slope)) with the center frequency f_c . The combined shaper bandpass is the stitched red curve with peak at 159 kHz.

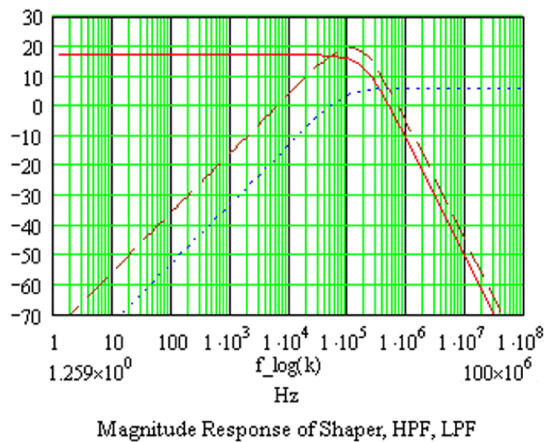


Figure 44 Transfer characteristics of the 2nd order PHOS shaper for a shaping time of 1 μ s. The center frequency is $f_c = 1\mu s/2\pi = 159$ kHz. The second order power damping above f_c is 40 db/ 10xf and the first order power damping below f_c is 20 db/10xf. The Nyquist frequency is the -10 db frequency point above f_c , i.e. ca. 500 kHz.

In the time domain, the shaper produces a semi-gaussian output signal with a peak voltage which is exactly proportional to the Voltage step of the CSP. The latter is proportional to the charge produced by the APD.

Figure 45 depicts the FEE analog signal filter which produces a semi-gaussian time response from a charge sensitive preamplifier (CSP) and a second order CR-2RC shaper.

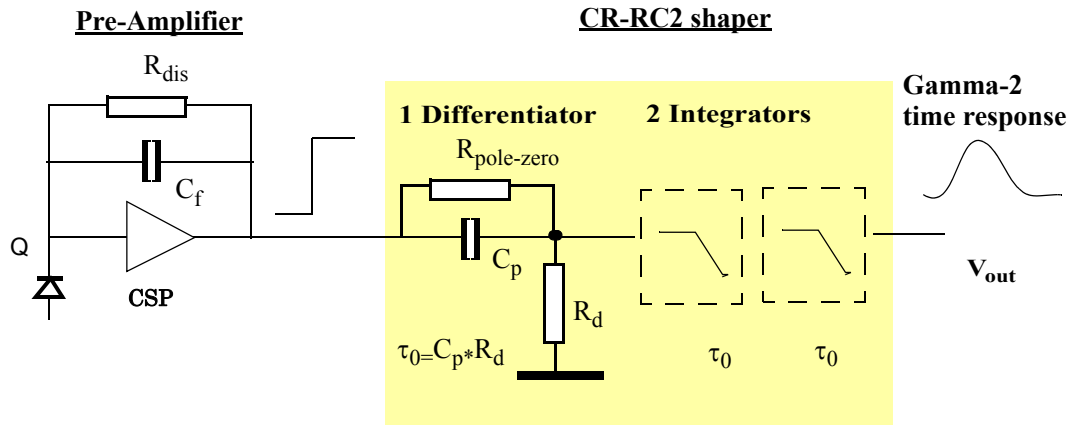


Figure 45 Semi gaussian shaper of type CR-2RC with pole-zero cancellation

With ($s = i\omega$) the Laplace function $H(s)$ of the above filter is shown in Equation 5. The transfer function for a step function s^{-1} is followed by the terms for differentiator, the CSP autodischarge term and the n^{th} order integrator. The time constant of both the differentiator and the integrators is τ_0 and A is the gain of the

$$H_{\text{shaper}}(s) = \frac{1}{s} \left[\frac{s\tau_0}{1 + s\tau_0} \right] \times \left[\frac{1}{1 + 1/(R_{\text{dis}} \cdot C_f \cdot s)} \right] \left[\frac{A}{1 + s\tau_0} \right]^n$$

CSP
CR differentiator
CSP discharge
RC integrator
step function
1-st order
term
n-th order

Equation 5 Not-compensated Laplace operator for the PHOS analogue stage

integrators and n is the order of the semi-gaussian shaper.

The autodischarge term of the CSP can be eliminated by adding the inverse “pole-zero” time constant

$$H_{\text{shaper}}(s) = \frac{Q}{C_f} \left[\frac{\tau_0}{1 + s\tau_0} \right] \left[\frac{A}{1 + s\tau_0} \right]^n$$

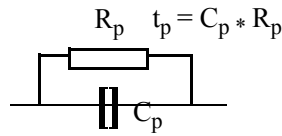
Equation 6 Compensated Laplace operator for the PHOS analogue stage

as depicted in Figure 45 via $R_{\text{pole-zero}}$ in parallel to C_p . The pole zero-cancellation consist in adding a RC network whose Laplace term of the form

$$1 + \frac{1}{R_f \cdot C_f}$$

Equation 7 Pole-zero term

This is simply an RC network as shown below placed



between the CSP and the shaper (see Figure 45). The time constant $t_p = C_p \cdot R_p$ should theoretically be equal to $R_f \cdot C_f$ (= 100 us), in practise, it has to be determined by experimenting.

By defining the peaking time of the output pulse is given by the shaper order n and shaping time τ_0

$$\tau_{\text{peak}} = n \cdot \tau_0 = 2\tau_0$$

The equivalence of the Laplace transform of Equation 6 in the time domain is a semi-gaussian pulse shape of form [36]

$$V_n(t) = \left[\frac{n^n Q \cdot A^n}{C_f \cdot n!} \right] \cdot \left[\frac{t}{\tau_p} \right]^n \cdot e^{-n \frac{t}{\tau_p}}$$

giving a peak amplitude V_{max} at τ_{peak} This equation shows that the peak amplitude V_{max} is proportional to

$$V_{\text{max}} = \frac{Q \cdot A^n \cdot n^n}{C_f \cdot n! \cdot e^n}$$

the charge Q produced by the APD.

For a second order shaper the time response function is a Gamma -2 function of the form:

$$V(t) = \left[\frac{2Q \cdot A^2}{C_f} \right] \cdot \left[\frac{t}{\tau_p} \right]^2 \cdot e^{-2\frac{t}{\tau_p}}$$

Equation 8 second order Gamma function for PHOS

5.1 Offline measurement of shaper signal

The choice of the PHOS shaping time τ_0 is 1 us as a compromise for low noise and timing resolution. The measured Gamma-2 shaper output as recorded offline is depicted in Figure 41

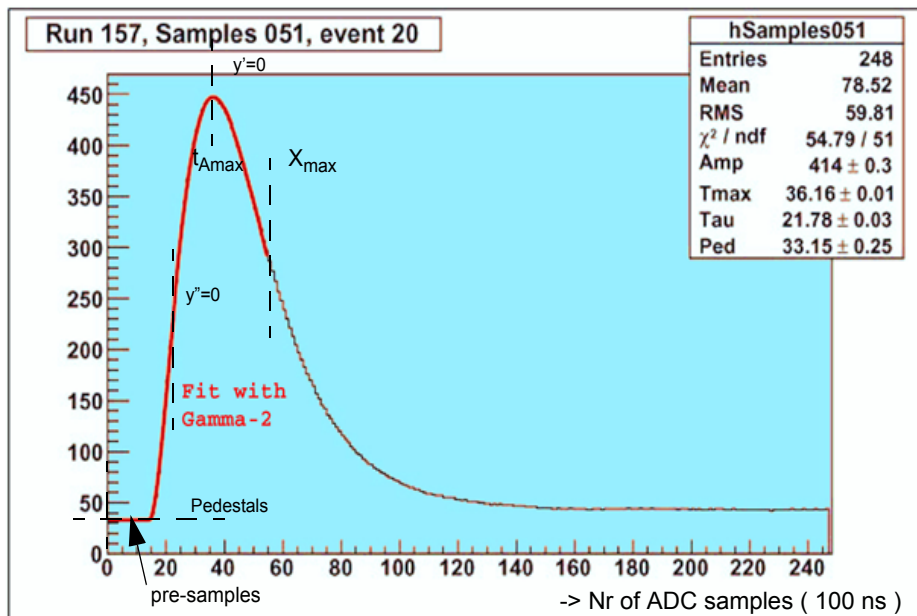


Figure 46 Output of Root Macro `shape.C()` showing the FEE shaper output in Alto ADC counts and as function of 100 ns samples for a Gamma-2 fit range ($X_{\text{max}}= 60$) in red. The signal was generated by a particle in the PW crystal.

The pulse returns to its pedestal level due to the proper pole-zero compensation applied in the FEE cards. It is very well described by the above Gamma-2 function which has the property that the timing reference of its first and second derivative are amplitude-independent.

Note: When fitting with Gamma-2, the fit should not extend beyond 1/3rd of the downslope like in Appendix 46, since otherwise the pedestals tend to "lift off"! This is due to the fact that the asymptotic downslope deviates from Gamma-2 due to the pole-zero-cancellation.

5.2 Measurements of peaking time τ

The shaper peaking time $\tau = 2 \times$ shaping time is obtained from the gamma-2 fit. To get the τ values for all channels, one can use the Root Macro:

.x get_TauAll.C(runNumber)

The shown measurement of (Figure 47 left side) was taken with a step pulse generator in the laboratory, hence is not undershoot compensated. The histogram (Figure 47 right side) shows the real τ value taken with LED pulsers. The two LED pulser points shown as blue points demonstrate that a 10 % increase of τ is the result of the pole-zero-compensation when using a voltage Step pulser.

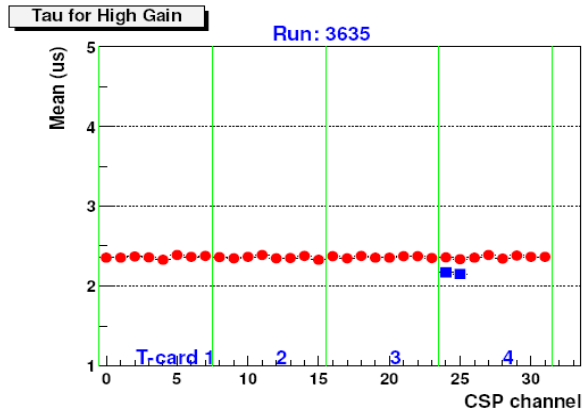
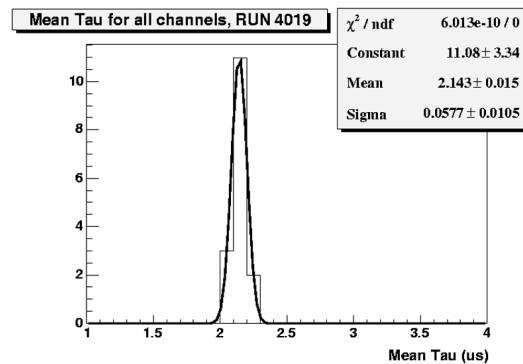
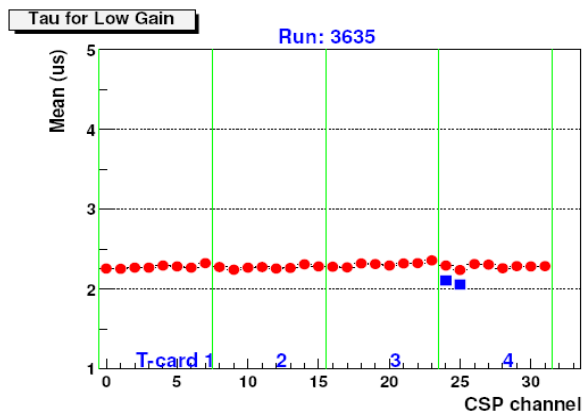


Figure 47 Left: peaking time τ for a FEE card measured by applying a step pulse to all shaper channels. The blue squares shown in the same plots are result with LED pulse to APDs of CSP channel 24 and 25 and lie ca 10% below.

Right side: The mean tau value measured with 8 LED channels is 2.14 us with a sigma of 0,057.



The shaper peaking time of FEE cards is 2.143 \pm 0.015 us

6 Cosmic particle detection with PHOS

Prior to commissioning PHOS in the ALICE experiment, PHOS was used for cosmic particle tests, triggered by a pre-version of the TRU trigger card, which set to low threshold (< 100 MeV).

The cosmic flux arriving at some altitude above the earth surface consists primarily of muons with a mean energy of 4 GeV at ground level and an almost flat energy spectrum below 1 GeV. The vertical flux is ca. 1 per cm^{-2} per minute. (see chap. 20 of [40]).

The flux of muons is 45 higher than protons and neutrons, 450 times higher than for electrons or positrons and 22500 higher than for pions. The Energy loss of Muons in PWO crystals was reported [33] as $dE/dx = 11.6$ MeV/cm.

The amplitudes of triggered cosmic particles over 24 hours in a 16 x 4 region of PHOS is shown in Figure 48.

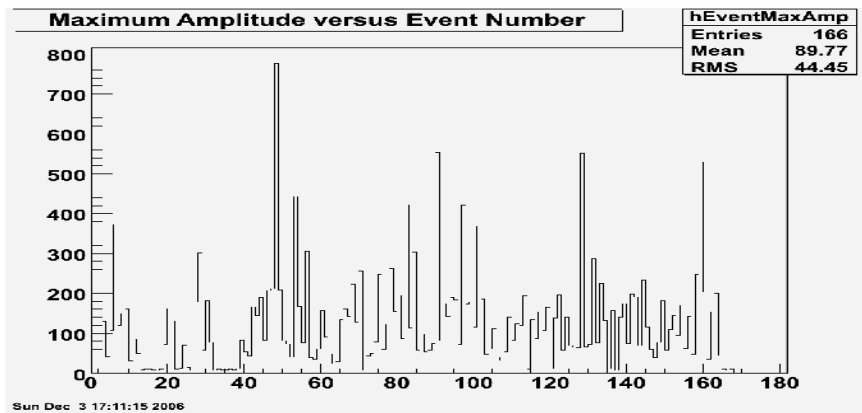


Figure 48 Cosmic Particle amplitudes in ADC counts, recorded over ca. 24 hours in 64 PHOS crystals.

Out of 166 triggered events, 9 events are of energy above 300 ADC counts (~ 1.5 GeV). The lego plot in the x-y plane of PHOS of the highest energy event (#48) is depicted in Figure 49. The total energy when summing up over all crystals is in the order of 30 GeV

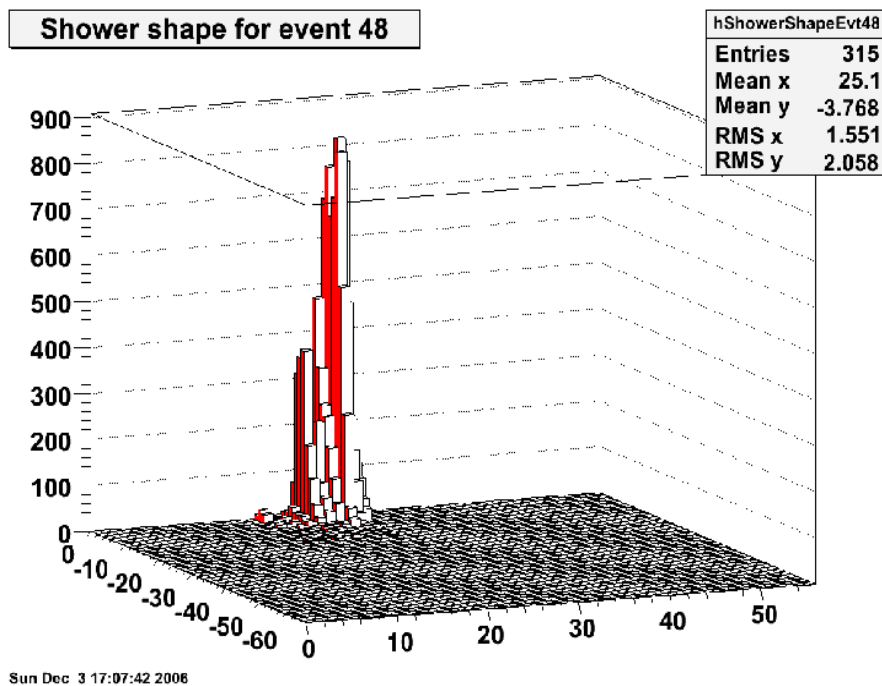


Figure 49 Lego plot of the hadronic shower event Nr #6. of cosmic run 5865

Figure 50 shows the passage of an un-identified cosmic particle through PHOS at room temperature and a

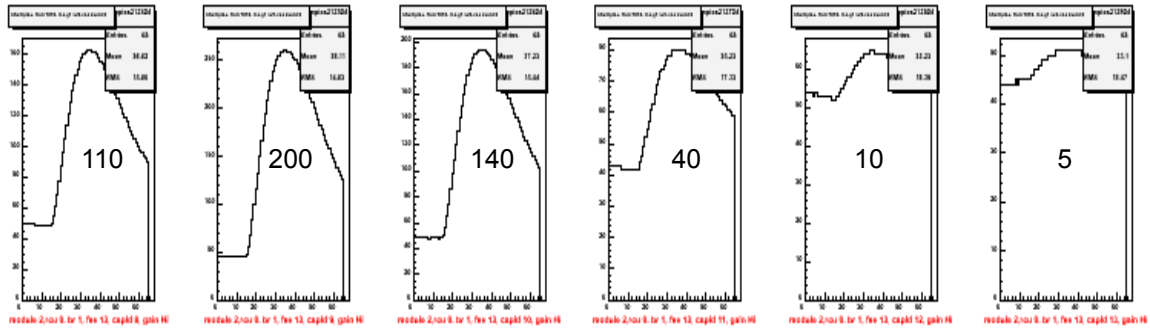


Figure 50 Energy deposit of a cosmic particle in 6 subsequent PWO crystals. The Numbers are the Energy equivalent peak ADC counts, corrected for pedestal offset. The angle of the particle relative to the PWO crystals is unknown.

nominal APD gain $M \sim 50$ (Hamamatsu value).

6.1 Punch through

Some of the events recorded in Figure 48 are due to punch through (nuclear counter) effect in the APD depletion layer. Minimum ionizing particles create ca 100 electron-hole pairs per μm of Silizium but only those in the depletion layer create an avalanche. PHOS has decided early on to replace pin diodes of the technical proposal [1] by APD diodes since the nuclear counter effect is much reduced in APD's due to a much smaller effective depletion layer (factor ~ 40) [42]. These parasitic events can be recognized since only a single channel is concerned without any shower distribution on neighboring channels. The most severe contamination is for measurement of MIP muons which have the same single channel hit signature. A punchthrough event is depicted in Figure 51. The single channel signature can be detected either online in the TRU trigger hardware

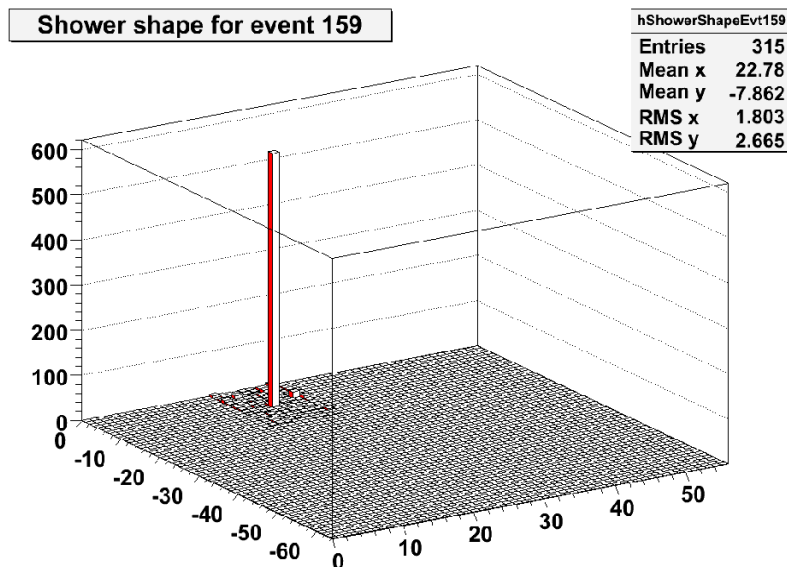


Figure 51 Fake single channel energy deposit due to punch through in APD

Sun Dec 3 16:53:24 2006

or in the offline trigger patterns.

6.2 Minimum Ionizing Particles (MIP)

Ionization loss by heavy particles is described by the Bethe Bloch Formula with a minimum of dE/dx stopping power between 100 MeV and 10 GeV for Muons. During the 2006 test beam, the PHOS

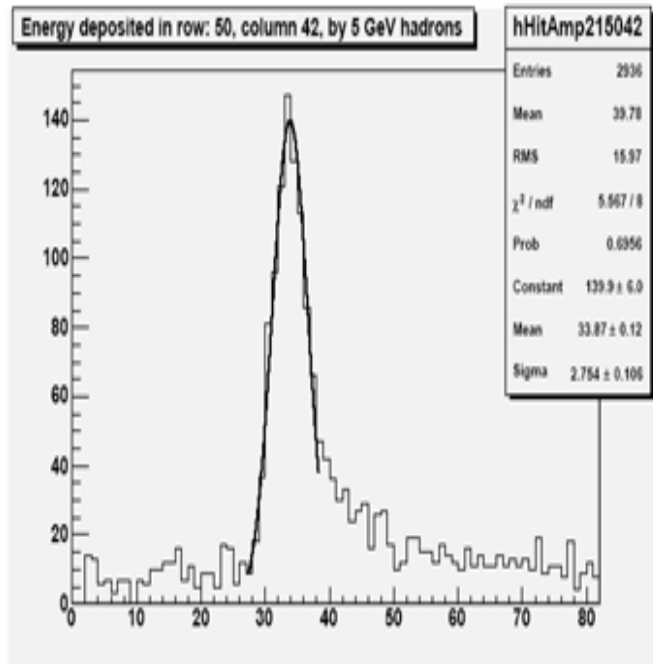


Figure 52 MIP peak with the PHOS detector during the 2006 testbeam with a 5 GeV trigger.

detector was exposed to a heterogeneous beam of particles with a differential Cerenkov trigger for particles within a selectable energy range.

The main composition included in the trigger of 5 GeV are Muons which generate the dE/dx MIP peak as shown in Figure 52. The resolution of the MIP peak is 8 %. The mean energy corresponds to ca. 34 ADC counts, estimated¹ as ca. 200 MeV @ -17 C. With 18 cm of crystals this would correspond² to 11.1 MeV/cm.

Note: The CMS value of dE/dx for PWO is 10.2 MeV/cm (room temperature) whilst the PANDA value is =13 MeV/cm hence this Measurement of 11.1 MeV/cm requires confirmation and may be 10% wrong. A precise measurement of the MIP peak with PHOS crystals at -25 C is still awaited as a very low energy reference of the energy calibration of PHOS.

1. This value can only be estimated since the data was taken during the 2006 testbeam at a cooling temperature of -17 C, corresponding to approx. 30% light yield compared to the nominal value 5MeV/ADC count.

2. The calculated dE/dx value of PWO is 9.4 MeV/cm, CMS quote 10.2 MeV/cm

7 PHOS geometrical

The PHOS photon spectrometer is an electromagnetic calorimeter consisting of PbWO₄ crystals with APD readout. Designed for the search of direct photons and π_0 and η production, PHOS consists of 5 distinct modules which are placed below the TPC inside the L3 magnet of ALICE with the following characteristic parameters

Geometrical: $\Delta\phi = 5 \times 20^\circ$, $\Delta Z = 1.26$ m, $R_{IP} = 4.6$ m

Pseudo rapidity coverage : $-0.12 < \eta < 0.12$

PbWO₄ crystal: $22 \times 22 \times 180$ mm³, $X_0 = 0.89$ cm, Moliere radius 2 cm, crystal weight 727 g

Nr of PWO crystals (FEE channels) $5 \times 3584 = 17920$

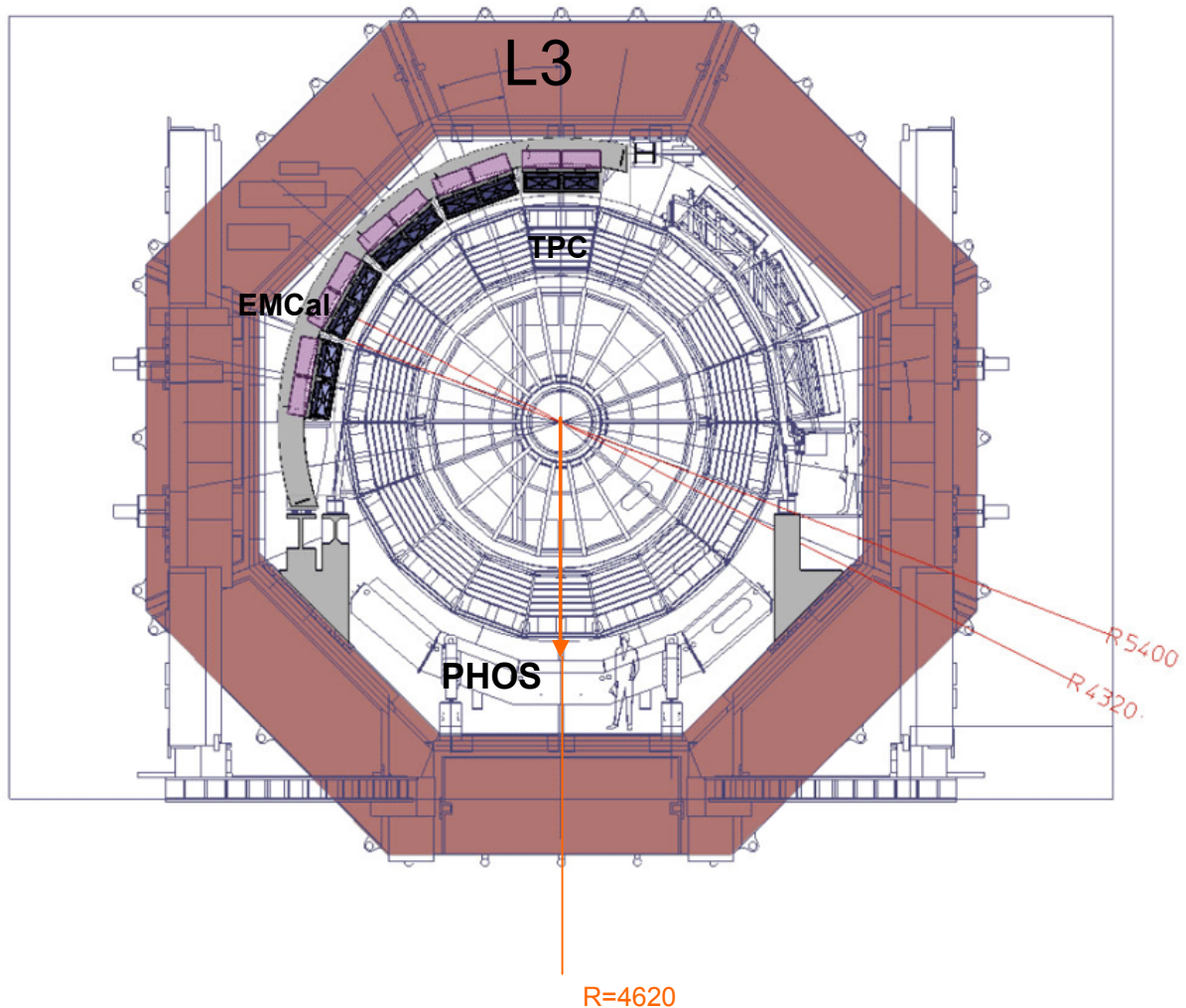


Figure 53 PHOS detectors inside the L3 magnet

7.1 Coordinate system

The global Alice coordinate system¹[37] is depicted in Figure 54. At the interaction point, the x coordinate points versus the centre of the LHC ring and with y pointing upwards, the right-hand coordinate system defines z in direction away from the muon absorber.

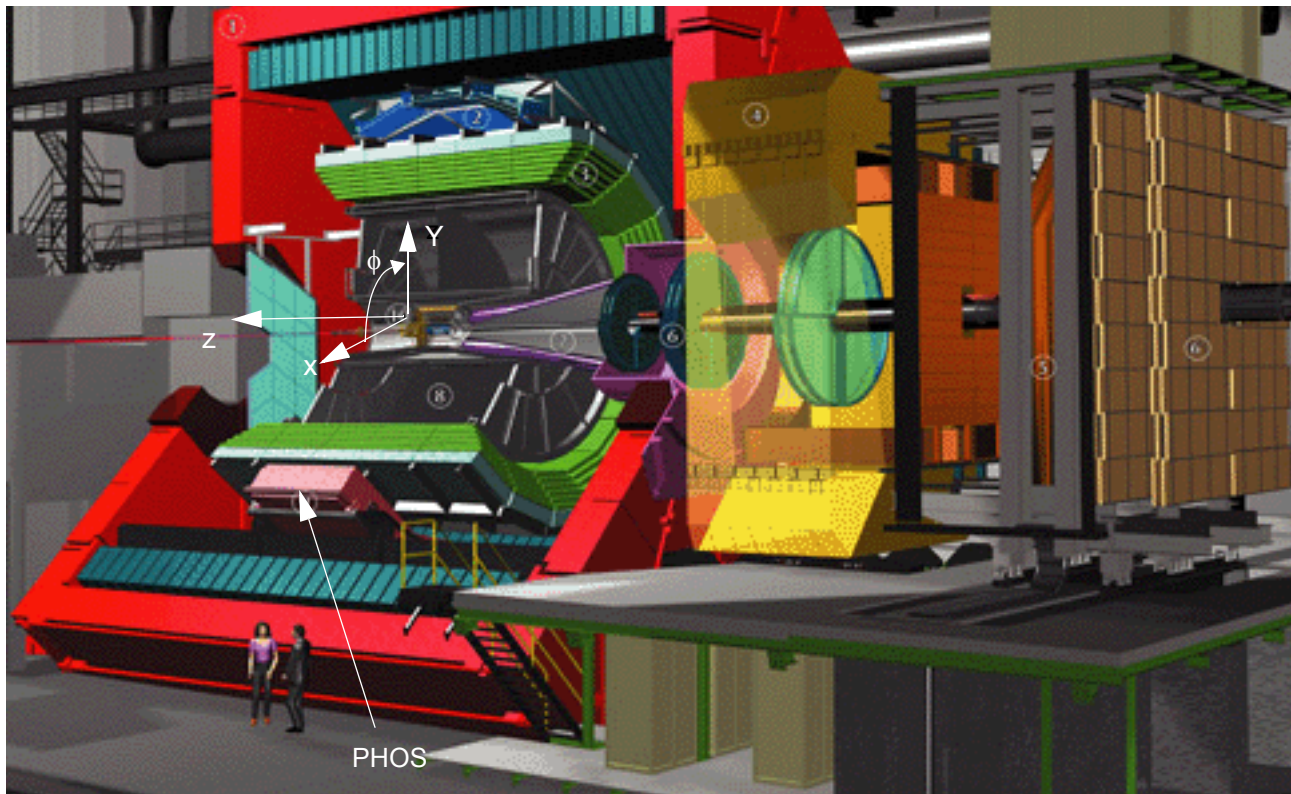


Figure 54 PHOS position within ALICE detector coordinates

The global Alice numbering scheme defines that

- rotational numbering increases with ϕ
- line numbering goes in **opposite** direction of z

1. defined in ALICE-INT-2003-038 and approved by the Alice Technical board. Note that the engineering coordinate system found on the Alice WEB pages under general layout is different. !

Figure 55 depicts PHOS module with its 5 individual PHOS modules. The 1st PHOS module installed in the

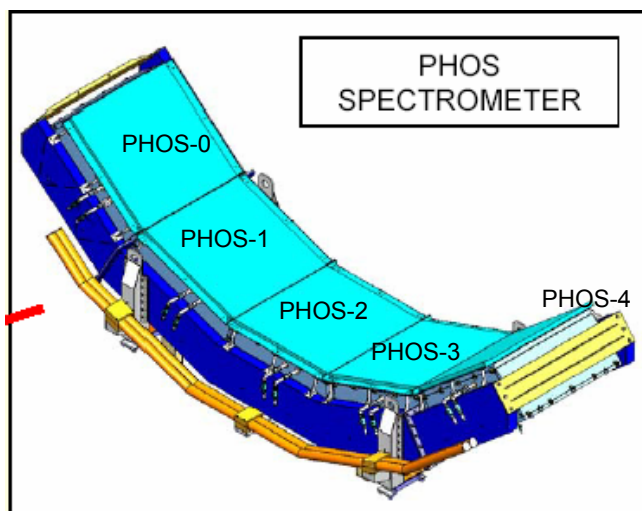


Figure 55 Arctic view of the PHOS detector

ALICE pit is PHOS-3.

Each PHOS module contains a matrix of 64*56 PWO crystals. PHOS is installed below the Alice TPC at 4620

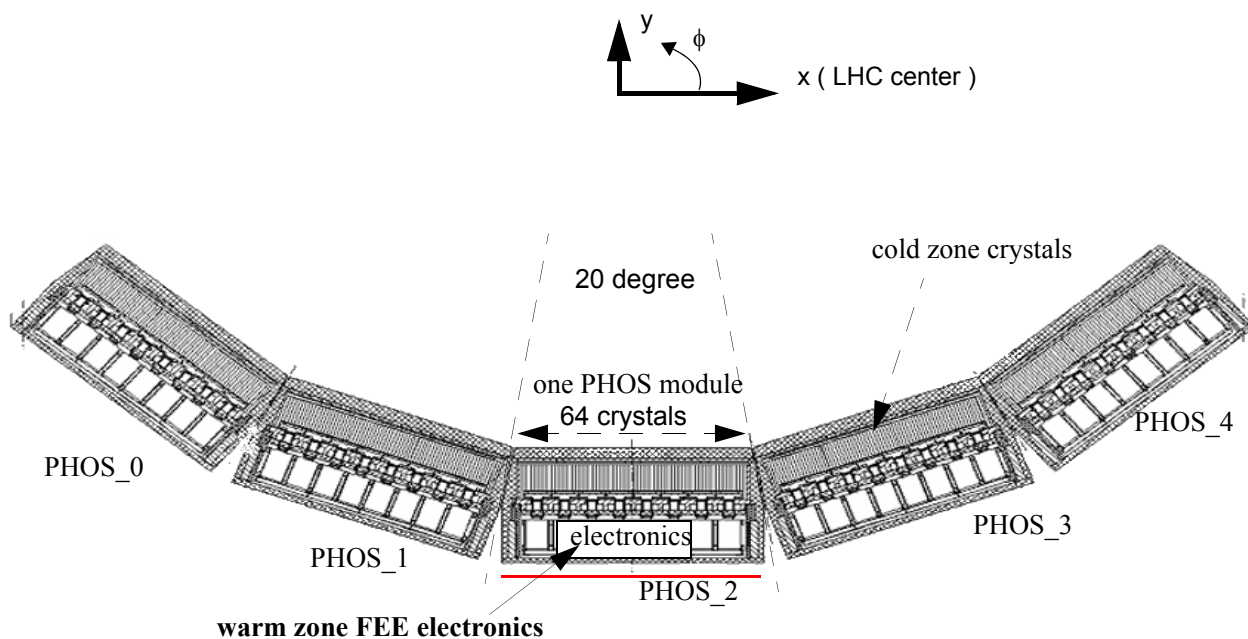


Figure 56 Arrangement of the 5 PHOS modules in z plane viewed from L3 Magnet door in direction GEX.

mm radial distance from the interaction point.

The first module built and tested and described in this manual is PHOS_2.

Each module maps with one TPC azimuthal sector in an angle of 20 degrees, corresponding to 64 PWO crystals of effective volume $22.55 * 22.55 * 180 \text{ mm}^3$. Each 20-degree sector length consists of 64 crystals and measures 1443 mm. A single crystal in the center of the module presents an angle of ± 0.135 degree towards the interaction point. The non-radial arrangement of the crystals per module implies a tilt of the incident photon angles up to max. 13 degrees for the crystals towards the degrees of the module.

A single PHOS module (turned into the y plane and viewed from the bottom electronics side) is shown in Figure 57. It represents a matrix of $56*64$ crystal. The (i,j) matrix corresponds geometrically to a matrix in x and z which

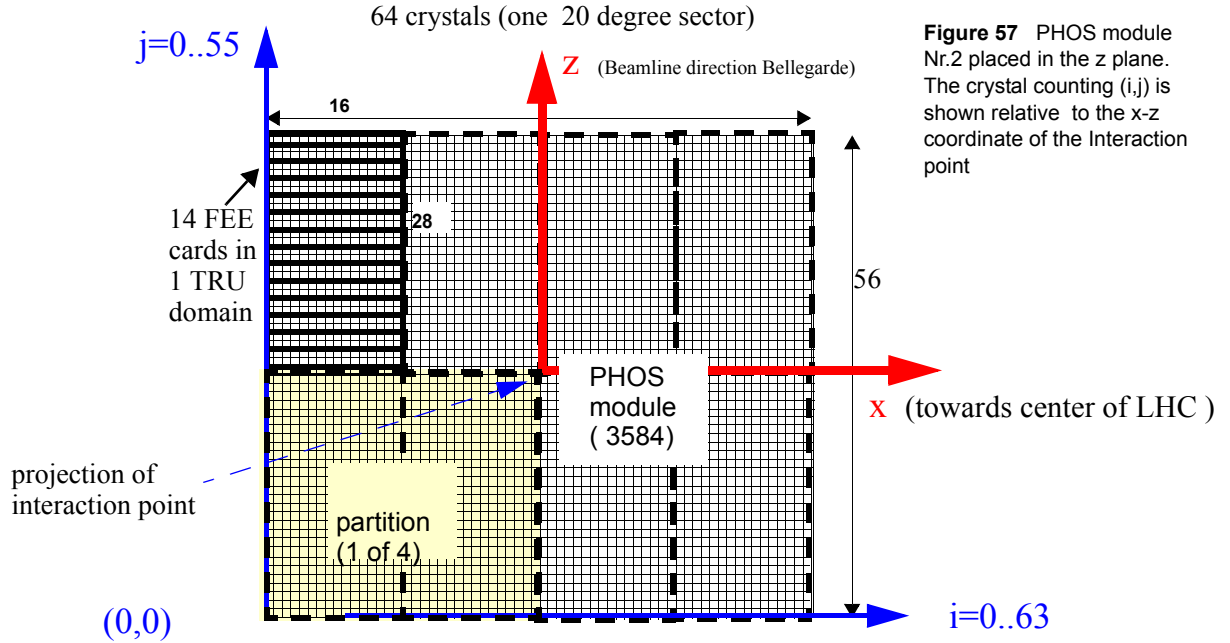


Figure 57 PHOS module Nr.2 placed in the z plane. The crystal counting (i,j) is shown relative to the x-z coordinate of the Interaction point

is divided in 4 RCU readout partitions, each containing $2*14$ FEE cards and 2 TRU trigger cards. The linear translation between the (i,j) crystal indices and the X,Z coordinates is

$$X = i + 32 * 22.55 \text{ mm}$$

$$Z = j + 28 * 22.55 \text{ mm}$$

Each RCU readout partition has 2 readout branches A and B and each branch corresponds to one TRU domain (Figure 57). The hierarchical nomenclature of PHOS is shown in Table 3

Table 3 Hierarchical Nomenclature of 1 PHOS module

1 FEE	1 RCU branch	1 RCU partition	1 PHOS module
32 input channels 64 readout channels each two 10 bit readout channels HG and LG	14 FEE cards 1 TRU card 448 input channels 896 readout channels	2 branches A+B 2 x 14 FEE cards 2 TRU cards 896 input channels 1792 readout channels	112 FEE cards 8 TRU domains 8 RCU branches 4 RCU partitions 3584 input channels 7168 readout channels 10 bit

The placement of the PWO crystals with their fixed CSP numbering (one CSP per crystal) in the ALICE coordinate system y-plane and relative to the FEE card electronics is depicted in Figure 59 below.

The fixed FEE card addresses increase in the z direction, CSP numbering increases in x direction.

Therefore the local address counting in PHOS goes in x,z. This requires that the placement of PHOS into the Alice global coordinate system as defined above requires a re-mapping of RCU partitions opposite to z.

The mapping of Alice x,y,z into local PHOS address is to make translations¹ between

(PHOS_Module, RCU_Branch, FEE_Address, Altro_Number, Altro_Channel) \Leftrightarrow (x, y, x)

- PHOS_Module: PHOS_0..4 increase in ϕ
- RCU_Branch: Branch_A and Branch_B increase in x
- FEE_Address: FEE_1 ... FEE_14 increase in z
- **(Note: The FEE address #0 is occupied by the TRU)**
- Altro_Number: Altro_0, Altro_2 increase in x at $z = z_0$
- Altro_3, Altro_4 increasing in x at $z = z_0 - 22.55$ mm
- **(Note: The Altro address Altro_1 is not implemented)**
- Altro Channel: Altro_0 = CSP 8,9,10,11 and CSP 24,25,26,27
- Altro_2 = CSP 0,1,2,3 and CSP 16,17,18,19
- Altro_3 = CSP 4,5,6,7 and CSP 20,21,22,23
- Altro_4 = CSP 12,13,14,15 and CSP 28,29,30,31
- **(Note: for details on FEE channel mapping see chapter 23.1)**

1. The index of PHOS mapping for PHOS_2 is given in <http://aliceinfo.cern.ch/alicevs/viewvc/PHOS/mapping/>

7.2 Electronics packaging inside PHOS

The FEE cards are mounted inside cooling cassettes which are open towards the upper power and bus connector side. The bottom side has holes for the frontside connectors which mate with the intermediate PCB towards the detector.

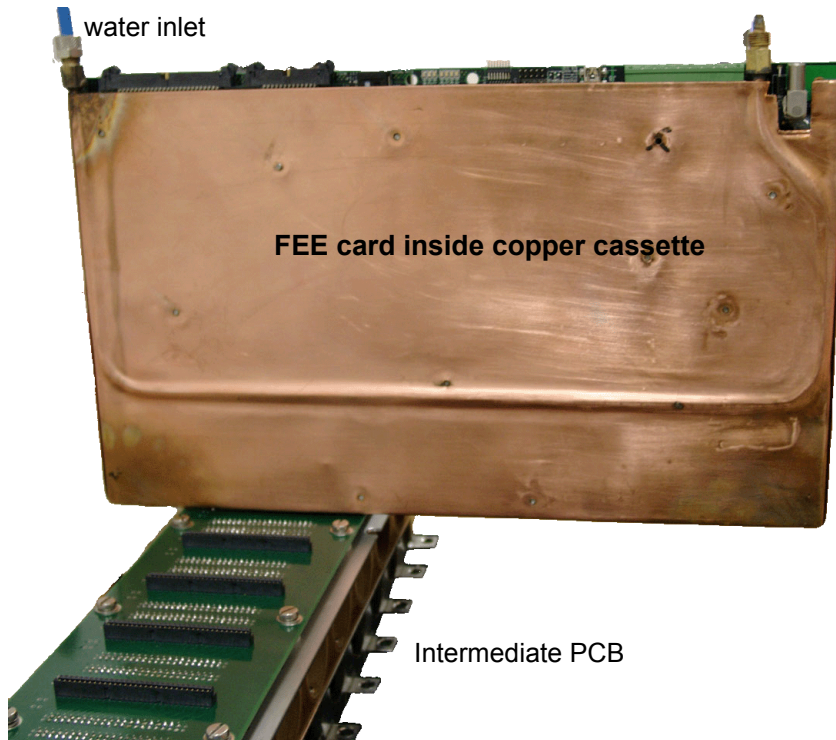


Figure 58 FEE card in cassette plugged on front side to intermediate PCB structure. The water inlet/outlet on the top correspond to the internal water pipe profile which is visible.

Note: in future PHOS modules the intermediate PCB structure will be replaced by a direct flat cable to the detector.

Figure 59 depicts the FEE and TRU positions and numbering of one of 8 RCU branches as viewed from the electronics side.

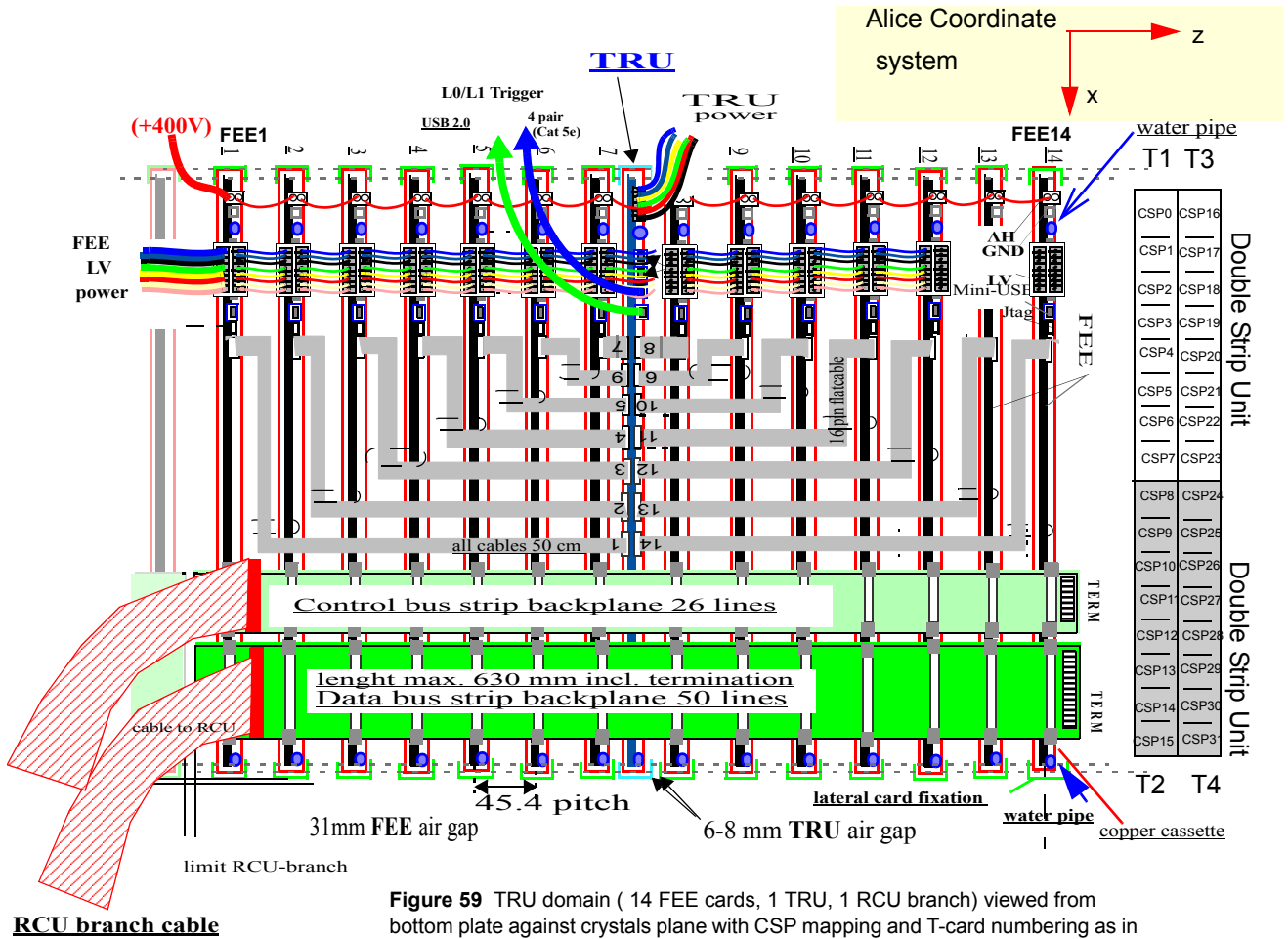


Figure 60 is a photo of the electronics side of the PHOS module consisting of 8 RCU branches and labelled in the local $i(x),j(z)$ coordinate system . In the final system, this view is covered by the PHOS bottom plate.

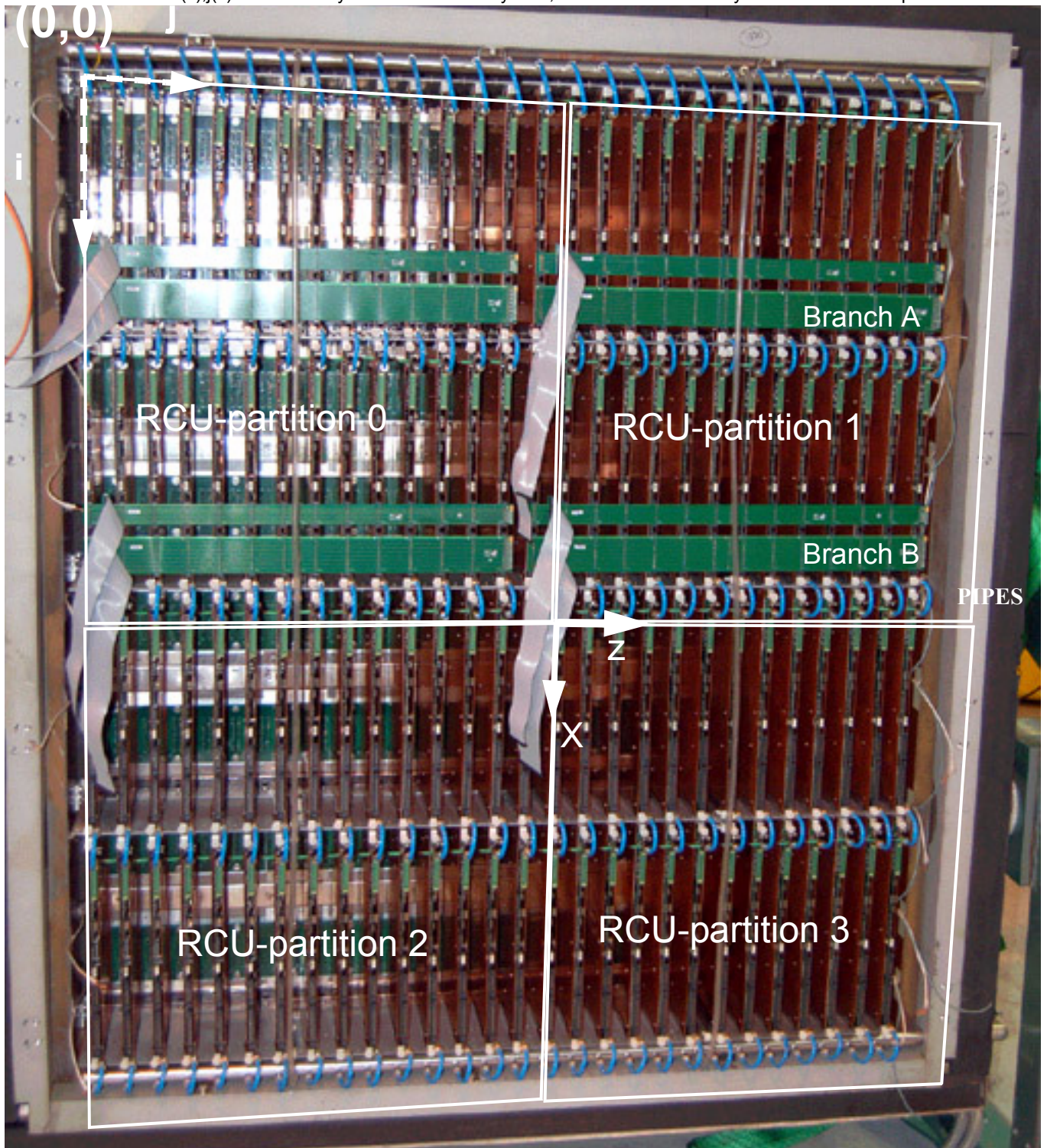


Figure 60 Photo of PHOS_2 electronics with bottom plate removed, the local coordinate system is superimposed

Figure 54 depicts the geographical position of the FEE and TRU cards within their RCU partitions. The crystal index i runs along x with $i=0..15$ per FEE card. The crystal index j runs along the beam direction z with $j=0,1$ per FEE card. The FEE addresses are hardwired on the GTL bus starting from decimal 1 (since the TRU's are placed at address 0) and ending at address 14..

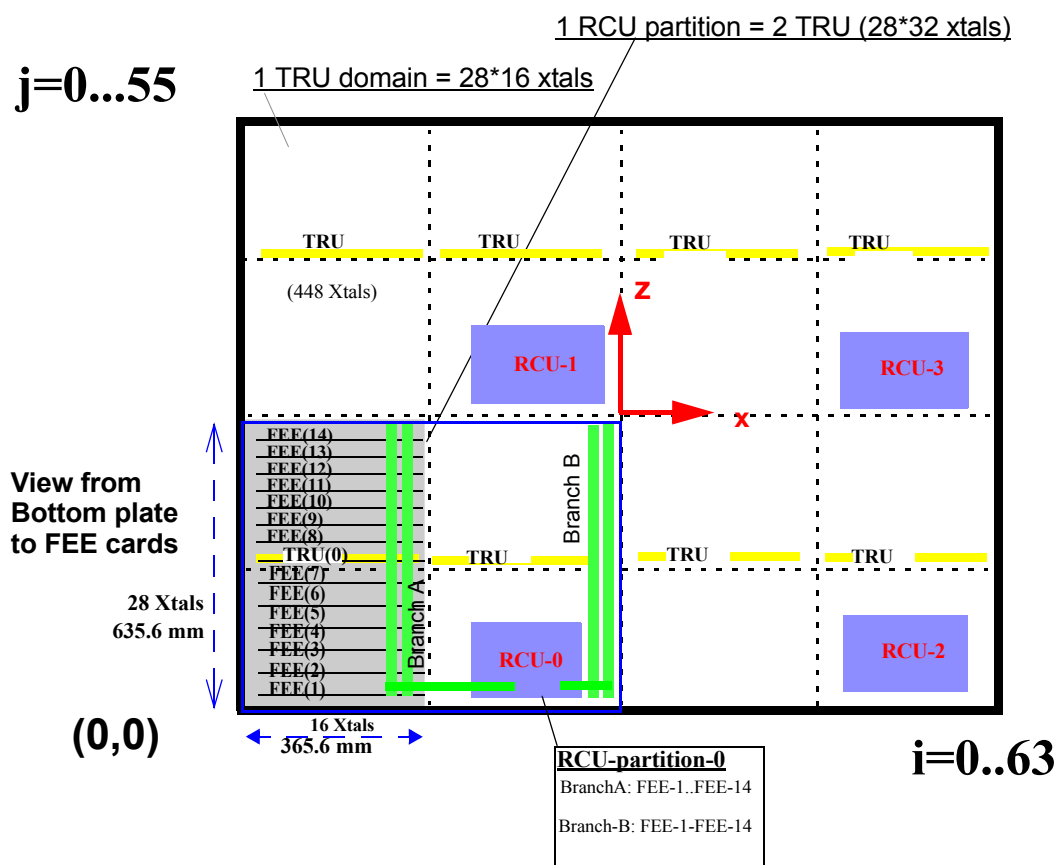


Figure 61 Fixed geographical FEE addresses and RCU numbering withing local x,y coordinate system

The detailed mapping of each FEE card relative to a double strip crystal unit is shown in Figure 182. The mapping of crystal/CSP addresses with Altro channels is defined in Figure 183

The PHOS control GUI display [27] is depicted in Figure 62 with superimposed x, z coordinates. All FEE cards belonging to RCU-1 are enabled on branch A and B and the readout configuration for RCU-1 is defined from x=0..31 and z= 28..55.

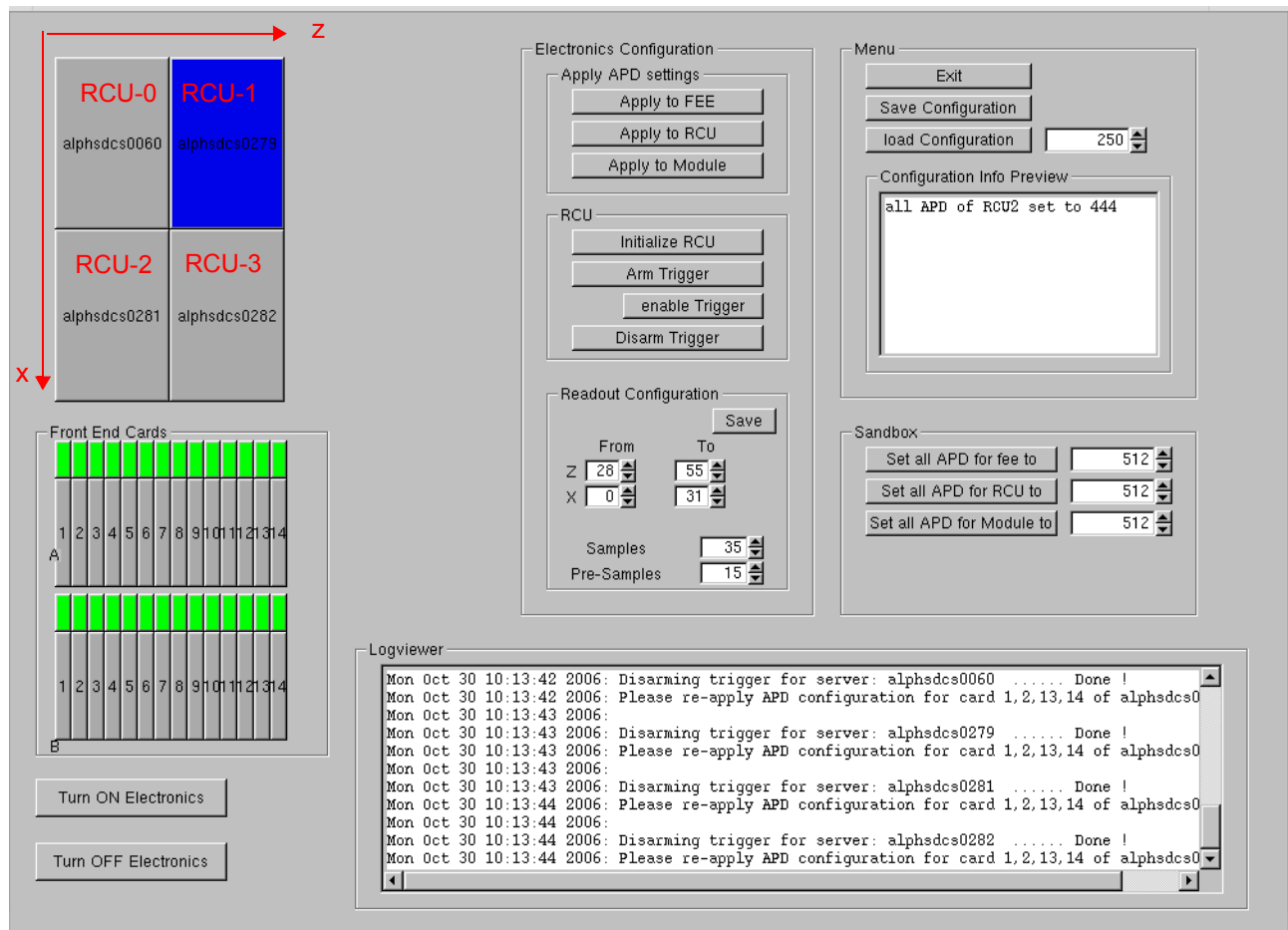


Figure 62 Screenshot of APD GUI for PHOS_2, for the readout configuration $j(z) = 28..55$, $i(x) = 0..31$

8 PHOS FEE Electronics overview

The FEE electronics main task is to measure the particle energy of each of its 32 channels very precisely over a linearity range of 16.000/1 (14 bit). The shapers produce a gaussian-like output signal (see Figure 36) which is Gamma-2 function compliant. A single channel is therefore composed of the digital samples of two shapers of gain ratio 1/16, each connected to a 10 bit Alto chip (see 8.6). The Alto's store ADC samples at the nominal sampling rate $f_s = 10$ MHz in it's Multi-Event-Buffer (MEB) whenever a level-0 and level-1 trigger pair is received.

The electronics overview plan of PHOS is depicted in Figure 63. The step voltage produced by each CSP preamplifier (see chapt. 3) is connected to a shaper(see chapter 5) on the FEE cards which filters frequencies below and above 160 kHz and therefore produces a semi-gaussian signal of 2 us peaking time which is digitized by the Alto chips [26]. The shaper has two output channels of different gains of ratio $A_1/A_2=16$. The gains are chosen such that 1 ADC bit of the high gain channel corresponds to 5 MeV and 1 ADC bit of the low gain channel corresponds to 80 MeV.

The 10 bit Altos ADC can sample the semi-gaussian pulse at frequencies up to 20 MHz. The maximum energy range for the high gain range of PHOS is 1024×5 MeV and 1024×80 MeV for the low gain range. The overlapping range between 5 MeV and 80 GeV represents a dynamic range of 14 bit. The digitized semi-gaussian signal shape of an event is stored in a Alto-chip-resident Multi-Event-Buffers (MEB). This storing is conditioned by successive trigger strobes L0 and L1, received via the Readout Control Unit (RCU) [18]. The number of samples and the trigger timing is defined by the configuration, sent by the DCS processor [2] (chapter 30) of the RCU. The recorded high- and low gain event data are sent by the Altos to the RCU whenever the RCU sends a Channel-Readout instruction via the GTL bus [see chapt. 12].

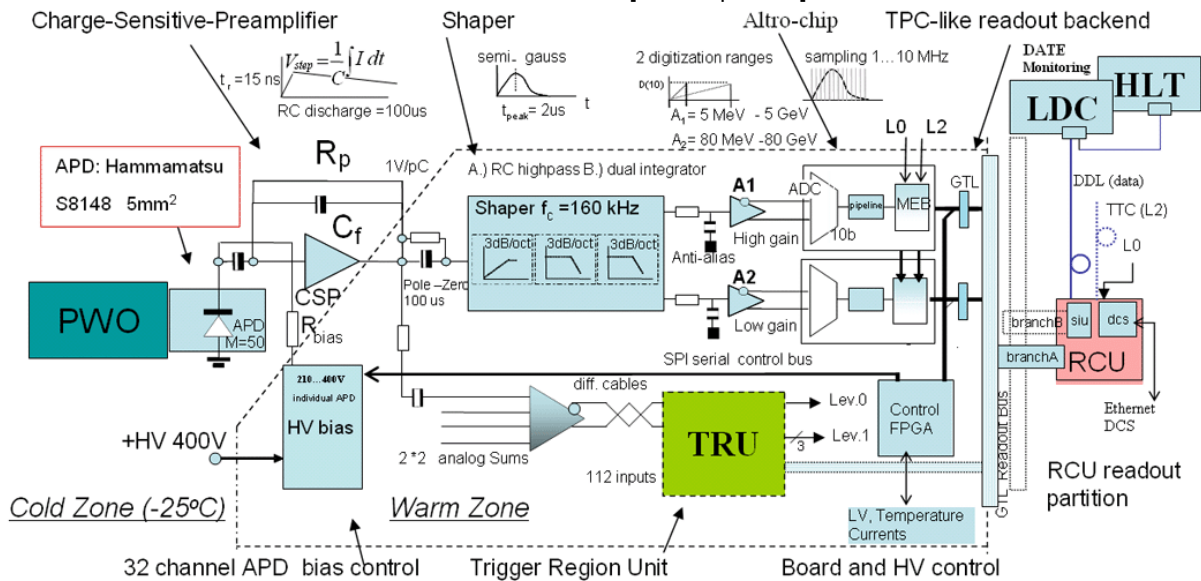


Figure 63 PHOS electronics global overview

The FEE electronics includes FPGA control logic for the PHOS Control and Monitoring referred to as PCM (see chapt. 15). This firmware package allows to configure all FEE parameters and to program the APD bias voltage of each CSP/APD channel. The PCM includes also a security module (see chapt. 15.4) which monitors voltages, currents and temperatures of FEE cards and generates interrupts of different severity levels if thresholds are overpassed. A custom, serial bus protocol between the RCU and FEE cards (see 15.7) insures that the security interrupts can be served at the same time when the 40 bit GTL readout bus is busy.

The RCU is controlled by the Detector Control System (DCS) and by the Trigger Timing Control (TTC). The RCU transmits event data to the Local Data Concentrator (LDC) which copies them to the High Level Trigger (HLT) farm. The transmission medium is the Alice DDL optical link.

The Trigger Region Unit (TRU) [40][41] will be described in detail in a separate document. A TRU receives 112 Fast OR signals generated by the FEE cards as analogue sums from 2x2 crystals. An analogue sum is generated from square 2x2 crystal channels via a simple quad CR-RC shaper which generates analogue output of 100 ns pulse width.

The Fast-OR logic (see chapt 21) generates 4 analog sums per double strip unit. With two double strip units (2x16 APDs) per FEE card, there are 8 Fast Or outputs per FEE card. The Fast Or signals are connected via 40 cm, differential cables to a central TRU trigger unit (TRU) which receives the Fast OR signals from 14 FEE cards.

8.1 ADC sampling

The shaper signal is permanently sampled by the Altro ADC, which passes the samples through a pipeline of max. 16 depth. At the output of the pipeline, i.e. after $t = 16/f_s$ the samples are lost unless a level-0 trigger is received by the Altro which enables the Altro logic to store a defined number of consecutive samples in one of its MEB buffers. If the level-0 arrives early enough, also pre-samples of the shaper signal are recorded. The pre-samples are important for measuring the "pedestal" level and the corresponding RMS noise of the signal in a single, coherent measurement. Taking noise measurements from pre-samples represents an unbiased measurement of pedestals and noise which requires however a fraction of the readout bandwidth. The minimum number of pre-samples is 8..10. By measuring pedestal noise in separate pedestal runs, an increased noise level is due to mixture with spurious noise.

The minimal sampling frequency f_s is linked to the Nyquist frequency, defined as twice the bandwidth of the shaper signal. For a shaping time $\tau_0 = 1$ us for PHOS, the input signal bandwidth (-6dB) is ca 500 kHz, for EMCal with 100 ns shaping time, the input bandwidth corresponds to 5 MHz. Therefore the minimum sampling frequency of PHOS is 1 MHz and for EMCal is 10 MHz.

The trigger timing for the signal readout is defined by the sampling frequency $f_s = 1/T_s$, the level-0 latency T_0 and the depth of the Altro pipeline (16). With a level-0 trigger latency $T_0 = 1200$ ns via the TTC link, the maximum number pre-samples N_p is:

$$N_p = f_s \times [16 / f_s - T_0] \quad \text{with } f_s \text{ in MHz and } T_0 \text{ in us.}$$

Example:

$$f_s = 10 \text{ MHz} \rightarrow N_p = 3$$

$$f_s = 5 \text{ MHz} \rightarrow N_p = 9$$

$$f_s = 2 \text{ MHz} \rightarrow N_p = 12$$

8.2 High and low gain

The voltage step signals at the output of the CSP are connected via IDC flat cables to the input of the FEE card.

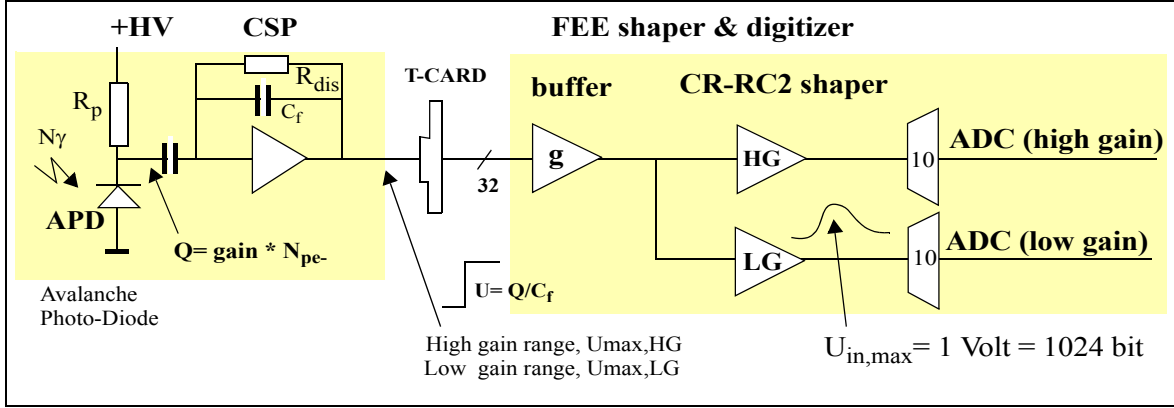


Figure 64 principle of front-end card

There are 32 APD channels connected to one FEE card. PHOS crystal channels or EMCal tower channels are mapped to the FEE cards via their dedicated T-cards(see chapt. 22). Each APD channel is split into HG and LG shaper channels with gain ratio 16/1, hence there are 64 shapers and 64 ADC's for the 32 channel FEE cards. With N number of samples the event-size readout channel is $2 * N * 10 \text{ bit}$. The readout bandwidth is discussed in chapter 11.6 .

The shapers of the FEE are implemented in discrete logic as 16 printed-circuit macros, each containing two pairs of HG and LG shapers. The Altro chips contain 16 ADC channels of 10 bit each. The Altro's 10 bit conversion range corresponds to an analogue shaper peak signal of ca. 1 Volt.

The PHOS/EMCal shapers on the FEE are user-configurable[34], discrete logic shapers of type CR-2RC, i.e. second-order shapers with the feature that the peaking time of the output signal is a factor 2 of the shaper integration time constant. The shapers are designed to reproduce almost exact Gamma-2 pulse shapes of the form

$$V_n(t) = \left[\frac{n^n Q \cdot A^n}{C_f \cdot n!} \right] \cdot \left[\frac{t}{\tau_p} \right]^n \cdot e^{-\frac{t}{\tau_p}}$$

Equation 9 Gamma function pulse timing function as solution for nth order CR-nCR shapers

with τ_p as peaking time, $n=2$ as order of the shaper and shaper-gain A. The maximum amplitude at $t = \tau_p$ is proportional to the amplified APD charge Q and therefore a linear measure of the scintillation light of one channel of the calorimeter, requiring that the APD gain is kept very constant over time and temperature. The time references ($y' = 0$ and $y'' = 0$) of the Gamma-2 compliant signal shape are amplitude-independent and used for offline Time-of-Flight determination.

The sampling rate used for all tests is nominally 10 MHz, it can however be reduced down to the Nyquist level which is defined by the shaper time constant and therefore different for PHOS and EMCal.

The maximum shaper signal amplitude at the input of the 10 bit Altro is set via a reference voltage to 1.0 Volt [see chapt 17]. With this the analogue value of 1 ADC count of a 10 bit ALTRO chip corresponds to

1 ADC count = LSB = 0.9765 mV

The Altro input is differential, hence measures a total analog swing of 2.0 Volt with hexadecimal output 0x000 for at 0.0 Volt of the signal. The center reference Voltage for FEE electronics is adjusted to 1.035 Volt (see Figure 146). This value includes a small offset above the zero-signal center value of 1.0 Volt for pedestal measurement (ca 35 ADC pedestal counts, see Figure 215).

The shaper gains are the signal amplification of the CSP Voltage step input relative to the peak of the semigaussian signal after the shaper.

The PHOS single channel energy scale is defined by the maximum channel energy = 80 GeV. By applying 10 bit ranges with a design gain ratio of 16/1, it follows with the definitions for 1 ADC count that:

$$1 \text{ ADC count (HG)} =: 5 \text{ MeV} \rightarrow \text{Max.} = 5.12 \text{ GeV}$$

$$1 \text{ ADC count (LG)} =: 80 \text{ MeV} \rightarrow \text{Max.} = 81.9 \text{ GeV}$$

By using the nominal CSP and Shaper voltages (for APD gain $M=50$) for 1 ADC count one obtains the design shaper gains:

$$\text{High gain: shaper gain}_{\text{HG}} = 6.85$$

$$\text{Low gain: shaper gain}_{\text{LG}} = 0.427$$

The real implementation does not need to reproduce these exact gain values since the assumptions about light-yield are only nominal and can be adjusted via the APD gains which are programmable on a channel-basis. Also the dynamic range is slightly changed from the design value if the gain ratio differs from 16.0 The offline determined value (16.84) is discussed in 8.5 and its consequences on the dynamic range in 1.4 .

A special feature of the FEE cards is that the bias voltages can be individually controlled by High Voltage logic on the FEE cards (see chapter 16.4). With a common input voltage of +400 Volt to all FEE cards, the programmable bias Voltage ranges from 210 - 400 Volt (0.1855 Volt per bit).

8.3 Charge measurement

With a charge capacitor of 1,2pF the CSP voltage/charge conversion gain $V = Q/C$ is:

$$0.833\text{V} / \text{pC} \text{ or } 0.133 \text{ uV} / \text{electron}$$

With the definition that 1 ADC count is set to 5 MeV for the high gain it follows (with 1ADC count = 0.9765 mV and with shaper gain = 6.5)

$$5 \text{ MeV} = 976\text{uV} / 0.133 \text{ uV} * 1/6.5 = 1129 \text{ electrons}$$

$$1 \text{ MeV} = 225.8 \text{ electrons}$$

$$1 \text{ ADC count} = 1129 \text{ electrons}$$

Further:

$$1 \text{ MeV} = 195.2 \text{ uV} \text{ (at the ADC)}$$

$$1 \text{ MeV} = 30 \text{ uV} \text{ (CSP output)}$$

8.4 Shaper gain

Based on the known pulseshapes of 2nd order CW shapers, a Gamma-2 function (Equation 9 for n=2) can be fitted to the ADC samples on an event-by-event basis. The information obtained from the fit is the peaking time $\tau=t_{Amax}$ and the peak amplitude $V(t_{Amax})$.

As shown in Equation 10 the peak amplitude($Y''=0$ derived from Equation 9) is proportional to the charge signal Q produced by of the APD and the shaper gain..

$$V(t_{Amax}) = \frac{Q \cdot A^n \cdot n^n}{C_f \cdot n! \cdot e^n}$$

Equation 10 Shaper pulse peak Voltage at t_{Amax}

With the CSP step voltage $V_{csp,step} = Q/C_f$, Equation 10 can be factorised as

$$V(t_{Amax}) = \frac{M \cdot Ne \cdot q}{C_f} \times \text{shapergain} = V_{(csp, step)} \bullet \text{shapergain}$$

Equation 11 Shaper peak amplitude depending on APD gain M and shaper gain

where Ne is the number of photoelectrons and M the APD gain.

Since 5 MeV corresponds by definition to 1 ADC count (0.976 mV), 1 MeV corresponds to 0.976/5= 1952 uV at the Altro.

The only variable parameter, the APD gain M, can be calibrated with particles such that

$$V(t_{Amax})/(MeV) = (0, 1952mV)/(MeV)$$

Equation 12 Shaper pulse peak voltage per MeV photons

With such calibration 1 ADC count corresponds to 5 MeV.

8.4.1 Shaper gain measurement with oscilloscope

The shaper gain is easily accessible to a direct ($\pm 10\%$) measurement: By using a triggered LED pulser the CSP preamplifier produces a step voltage which corresponds to a shaper A_{\max} amplitude. Figure 65 shows a simple, *shapergain* measurement using an oscilloscope to measure the LED pulse, the CSP step Voltage

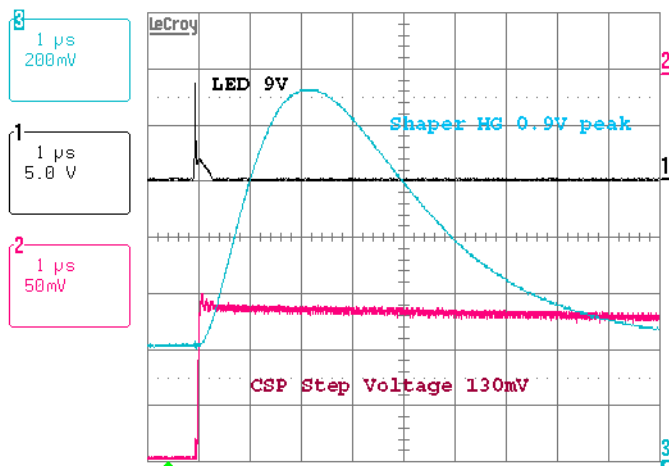


Figure 65 Oscilloscope measurement of **high gain** shaper with LED pulser. The 2 us CW shaper gain with 130 mV CSA input and shaper peak amplitude of ca. 0.9 Volt corresponds to $gain_{HG}=6.9$

and the corresponding shaper amplitude.

The gain ratio obtained by this simple measurement with LED pulser as $V_{Amax}/V_{CSP-step}$ is

$$shapergain(high gain) = 6.9$$

$$shapergain(low gain) = 0.42$$

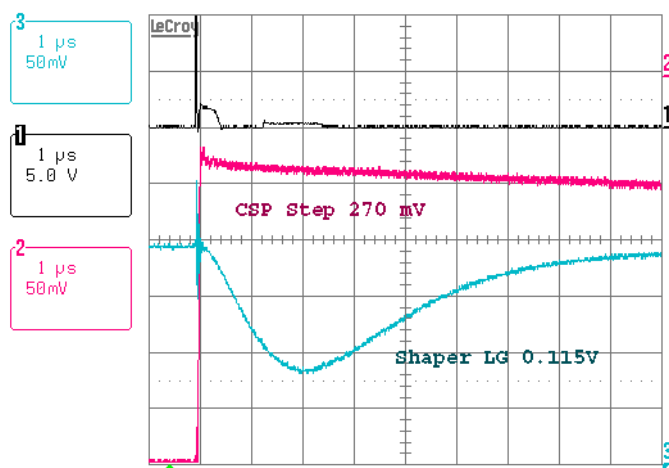


Figure 66 Oscilloscope measurement of **low gain** shaper with LED pulser. The 2 us CW shaper gain with 270 mV CSP input and shaper peak amplitude of ca. 0.115 Volt corresponds to $gain_{LG}=0.42$

The gain ratio obtained in this simple way is 16.43. This value is not far from the precise value obtained by an offline measurement with many events.

8.5 Offline shaper gain measurement

The offline measured gain ratio distribution over 32 channels with LED pulser and APD at -25 C is depicted in

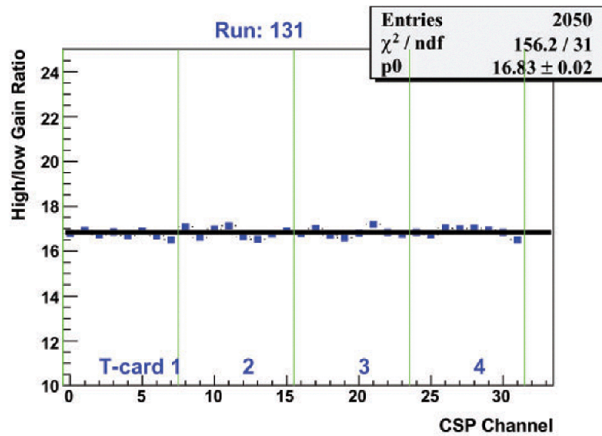


Figure 67 Shaper gain ratio over 32 FEE channels.

Figure 67 for 2050 events. The statistically obtained value is:

$$\text{HG/LG} = 16.83 \pm 0.02$$

The effect of this number which deviates slightly from the target value of 16.0 is that the dynamic range is slightly increased.

8.6 Altro ADC [26]

The ALTRO-16 chip¹ [26] of the ALICE TPC is also used by the PHOS FEE for digitization and processing of the semi-gaussian pulseshapes of the FEE shaper. The Altro chip contains sixteen 10 bit ADC's, each followed by a signal processing chain and up to 8 MEB event-buffers. The Altro chip is produced by ST Microelectronics, based on a 0.25 μm HCMOS process, consisting of ca. 6 million transistors and sold in a TQFP-176 package. With a supply Voltage of 2.5 Volts it's power consumption is 15 mW per ADC channel. Shown in Figure 68 is one of its sixteen 10-bit ADCs blocks, followed by a processing chain and the Multi-event buffers. The common control logic contains registers, the readout bus interface and the trigger manager.

1. produced by ST Microelectronics

The Multievent buffer (1040 * 40 bit) can be partitioned into 4 or 8 event buffers.

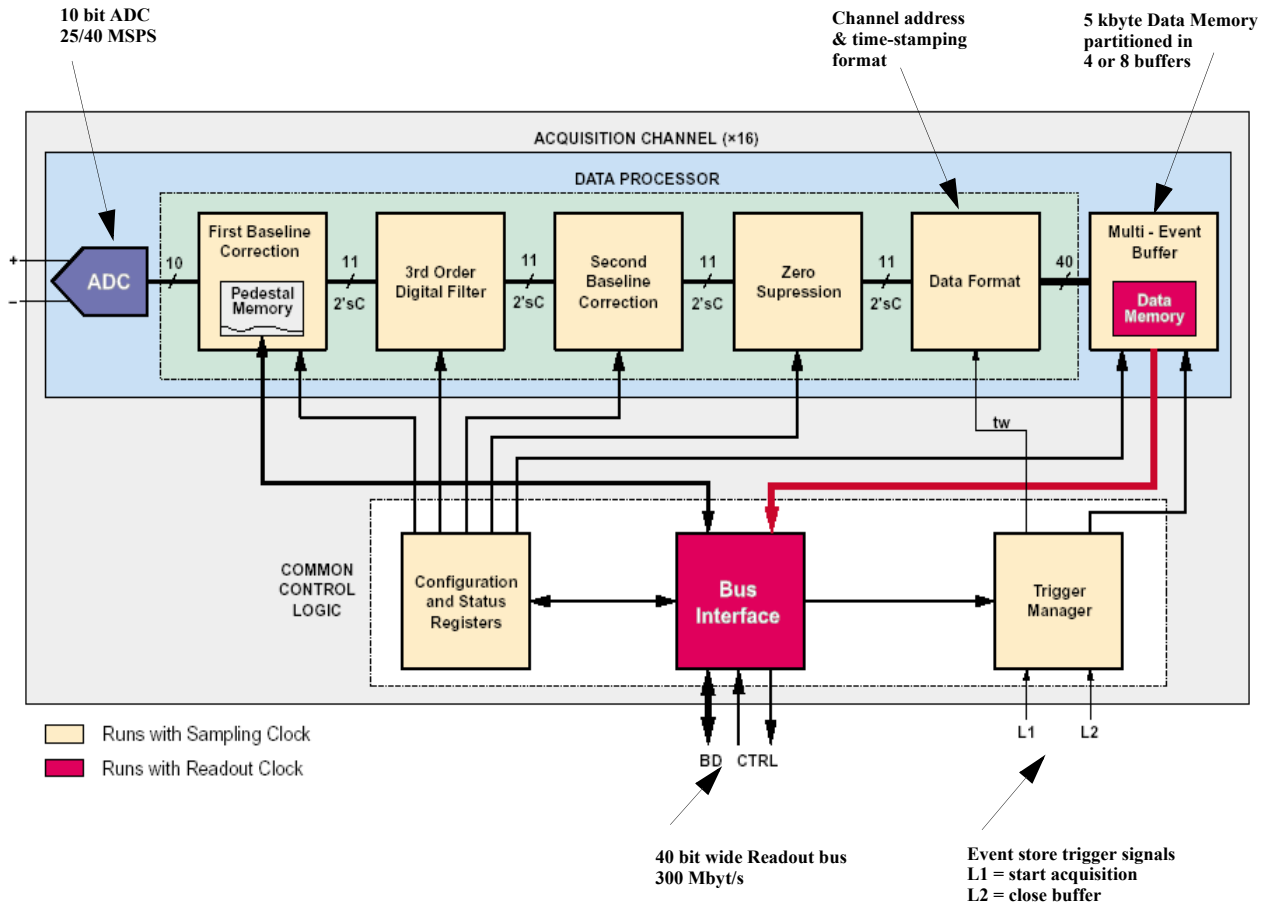


Figure 68 Block diagram of the Alto-16 chip (From Alto Manual) showing one of 16 ALTRO channels.

The data readout requires a GTL interface to the LVTTTL interface of the Alto chip. This is implemented using GTL transceivers in an ALTRO compatible mode, i.e. the GTL drivers GTL16612DGG are operated at 2.5 Volt supply voltage (though they are specified for 3.3 Volt !).

The A/D converters are based on the TSA1001 macro block made by STMicroelectronics which can be clocked up to a maximum of 40 MHz. As depicted in Figure 69, depending on the input signal bandwidth the number of effective bits (ENOB) is reduced below 10 bit. At the PHOS Nyquist frequency of 1 MHz, the number of effective bits (ENOB) is 9.7. The ADC data are transferred at the sampling rate into a 6 stage data processing pipeline which can perform a baseline subtraction, a tail cancellation filtering, adaptive baseline correction, and zero suppression. Groups of four ADC filters input their 10 bit data via a 40 bit bus into the embedded multi-event

buffer. The strobes L1 and L2 for storing data into the Multi-even buffer have to be provided externally by the trigger system. There are 3 trigger modes which can be defined in the TRCFG trigger configuration register (see 30.10 .) The 40 MHz output bus is clocked at the 40 MHz readout clock rate, resulting in a peak burst bandwidth of 200 Mbyte/s at which the Altros transmit individual buffers to the RCU.

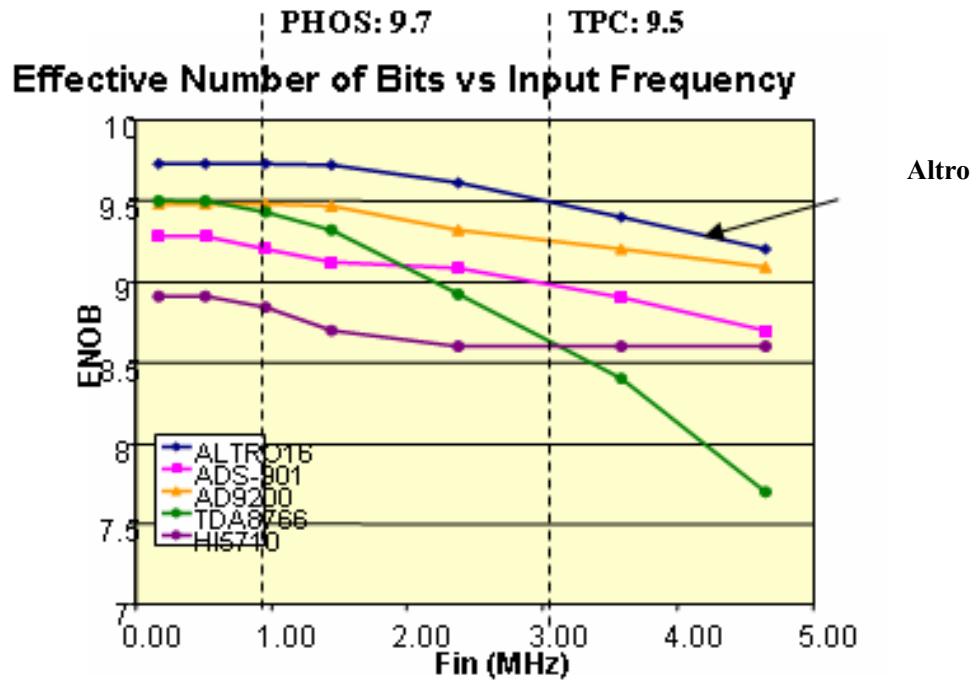


Figure 69 Left: Effective Nr of bits vs sampling frequency of the ALTRO chip [27]. Right: Effective Nr of bits vs input Bandwidth (shaper) for several ADC's and Altro [28]

The sampling rate is in principle freely selectable (at the RCU level) between the Nyquits frequency and a maximum Altro sampling frequency of ca. 25 MHz. With a shaper bandwidth of ca. 0.5 MHz, PHOS applies overclocking above the Nyquist frequency of 1 MHz.

In test mode, the output of the Altro ADC's is directly available on the output bus, see 15.8 .

8.7 Summay of FEE electronics parameters for PHOS

APD Light yield @ -25 C for a nominal PWO(+25C) Lightyield of 10pe/MeV and gain=1

-> 4.4 photo-electrons /MeV

APD light yield at nominal **APD gain 50:**

-> 220 electrons/MeV

Preamplifer: **charge / Voltage conversion factor:**

$U=Q/C$ with $C = 1.2$ pF CSP output = 0.133 uV / electron

Shaper gain high = 6.9

Shaper gain low = 0.42

ADC count equivalence to preamplifier output:

$$1 \text{ ADC count high} = 1/\text{shaper gain} * 1\text{V}/1024 = 0.142 \text{ mV (CSP)}$$

$$1 \text{ ADC count low} = 1/\text{shaper gain} * 1\text{V}/1024 = 2.28 \text{ mV(CSP)}$$

RMS noise (from presamples @-25 C) = average 0.262 ADC = 37 μV

Electron Noise equivalent:

$$37 \text{ } \mu\text{V} / 0.133 \text{ } \mu\text{V} = 278 \text{ electrons}$$

Dynamic range

5 MeV .. 81.2 GeV (14 bit)

1.) high gain (10 bit) 5 MeV - 5.1 GeV

2.) low gain (10 bit) 80 MeV - 81.9 GeV

1 bit = 5 MeV

Noise:

RMS noise (measured 0.262 ADC count single channel RMS = 1.28 MeV

The RMS noise of an EM shower (3*3 crystals) $3 \times 1.28 \sim 4 \text{ MeV}$ (3x3 noise term)

Note: these Noise values have been measured in the laboratory with old crystals in a -25 C freezer. The noise in the real PHOS module may be more due to a less-ideal grounding and crosstalk environment.

9 FEE card

The PHOS FEE card features fully linear 14 bit dynamic range shaper electronics of very low noise with analog fast or trigger outputs and novel, high precision APD bias control per channel on a single PCB. The CERN/Wuhan shapers (CW) were specially developed for the PHOS requirement to achieve a low noise term of less or equal 10 MeV and to provide an amplitude independent peaking time for offline time-of flight determination in the order of 1.5 ns. The RCU readout backend and Altro bus protocol was adopted from the TPC. A USB port provides for diagnostics without RCU backend¹. The first 32 channel FEE card version 1.0 was designed at CERN and produced in Wuhan in 2004; it was successfully tested in the October 2004 testbeam at CERN and revised for lower noise in January 2005. Revised prototypes (Rev.1.1) were produced in Wuhan in June 2005 and used for extensive laboratory testing. A derived version with 200 ns peaking time was tested successfully in an EMCal test beam at Fermilab in Nov. 2005. EMCal features about the same light yield as PHOS but uses FEE cards with shorter peaking time and at a higher energy range (16 MeV - 250 GeV) and operate at APD gain $M=30$ at room temperature. The FEE electronics for the first PHOS module (7168 readout channels) is based on the FEE Revision 1.1a, which was produced in Wuhan in December 2005 and delivered to CERN in January 2006. Throughout 2006 this electronics was used for commissioning the first PHOS module in the 2006 testbeam at the PS. The electronics for the following 2 PHOS modules requires a slight revision referred to as FEE1.1b which will be produced, tested and shipped to CERN by May 2007 by the Chinese team. The first EMCal FEE version with 200 ns peaking time will be produced at the same time and is referenced as FEE1.1e.

FEE1.0 2 us shaper (4 us peaking time) 2005 used with the PWO matrix in testbeam 2004

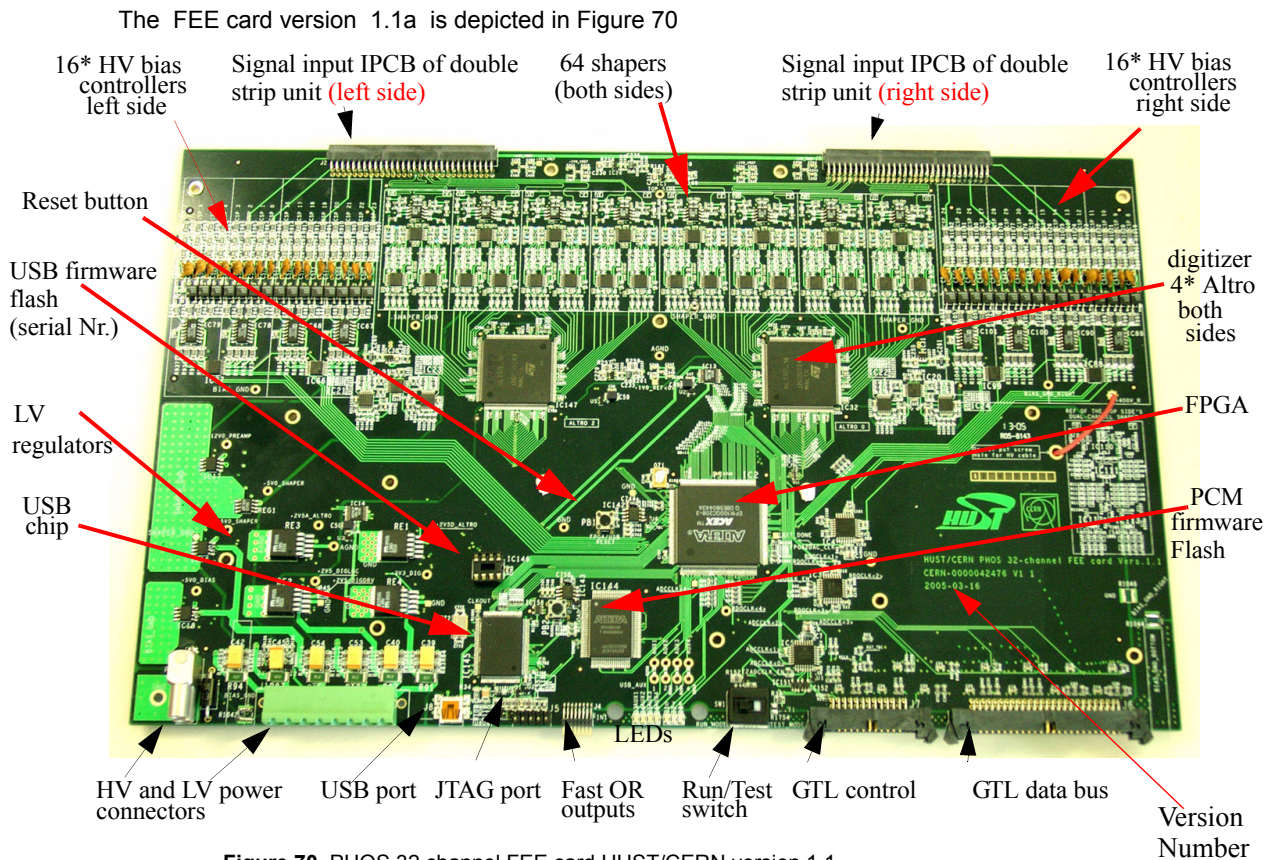
FEE1.1a 1 us shaper (2 us peaking time) 2006 used with the 1st PHOS module in testbeam 2006

FEE1.1b 1 us shaper (2 us peaking time) USB removed, Test mode removed, input connector for adapter for next PHOS 2007

FEE1.1e 100 ns shaper (200ns peaking time) USB removed, Test mode removed, LS2 input connector, for EMCal

This user manual was compiled during the tests of FEE v1.1a and commissioning of the first PHOS module until July 2006.

1. thips option was removed in recent FEE versions 1.1b, 1.1e



The FEE card firmware (PCM) is programmed into a Flash memory (via the JTAG port, alternatively also via USB) and on power-on, the Flash the firmware is loaded in the FPGA. A reset button on the FEE card allows also for manual resetting.

9.1 USB functionality¹

The USB port functionalities on the FEE card have been under development up to FEE 1.1a. The thesis of 2004 by J.Vallaey's [10] describes the basic concepts in great detail. The USB controller is connected to the PCM by a bidirectional FIFO data port and by the I2C serial bus which also connects to the USB Prom.

The I2C driver and USB utilities were intended for communication between the USB prom and the PCM (see Figure 113). The target of the USB functionalities on FEE 1.1a is restricted to FEE testing, i.e. to give access to PCM registers, including bias control registers. The serial number of FEE cards is contained in the serial USB prom and can be read via the PCM register at 0x70, using implicitly the i2c connection to USB. It was planned that programming of the APD bias voltages could also be performed via the USB port.

The USB test mode without RCU requires that the test switch on the FEE is set to test. In this case the sampling clock and the readout clock are generated by the PCM. The PCM functionality is initially restricted to set and / or read PCM registers, including bias registers.

1. The USB support chips will be removed from FEE 1.1b and FEE 1.1e

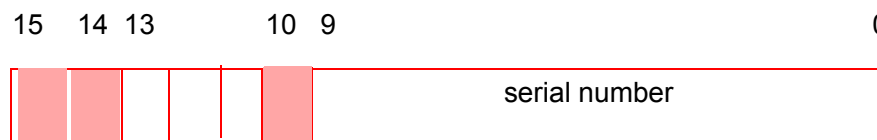
Note: in order that PCM works in test mode on FEE 1.1a without GTL bus and RCU, the reset of the GTL bus (RST_GT, see Figure 108) is unfortunately permanent and requires a pullup resistor of 1 K to 2.5 Volt. Subject for future FEE revisions: remove the reset status without GTL bus by a test jumper .

9.2 PCM versions and FEE serial Numbers

The PCM firmware is described in chapt. 15 .The current FPGA firmware version is PCM 2.0 [9]. PCM firmware updates become available in the course of time [14].

The PCM version number is stored in the register at 0x20. For the version PCM 1.2 the register content is 0x12. The binary PCM files for programming the FPGA and the Flash have the extension .sof and .pof

The **FEE serial Number** is a 16 bit word stored in PCM register (0x70 and 0x71) have the following format:.



- bits 0-9 bits are the serial number (Note: on the label, this number is decimal)
- bit 10 is reserved (default is 0)
- bit 11-13 are revision number
- bits 14-15 designate the detector (01 for PHOS, 10 for EMCAL)

An example script to read the serial number via the DCS card shell utilities (see chapt. 18) at PCM address 0x70 is shown below as execution of the script "get_serial_no_s4.scr".

```
[enter operation (h/i/q/r/w):b get_serial_no_s4.scr
executing: w 0x7000 0x524070      # read from branch A ,address4 Register 70
executing: w 0x7001 0x0390000     # terminate command list
executing: w 0x0 0x0              # execute command starting from address 7000
executing: r 0x6000 1             #read result register, 1 word
0x6000: 0x4806                   # result
```

Decoding serial Nr. 0x4806=

01.00 1.0.00 0000 0110

PHOS. Rev. 1. Serial No = 06

The register 0x70 reads the serial number from the USB EEPROM, i.e. by programming of the EEPROM via the USB port, the serial number can be changed. The register 0x71 reads the serial number which has been programmed into the PCM firmware.

9.3 Technical Documentation

The PHOS FEE schematics of version FEE V1.1a including the component lists, this user document and other documentation is available under the CERN EDMS Database

<https://EDMS.cern.ch> -> / ALICE/ Alice Engineering Baseline/ ALICE PHOS FEE .

The hierarchical design schematics have been generated under the CERN Cadence Concept licence, as well as the corresponding component list for the PCB mounting machines (Bill Of Materials = .bom files).

9.4 PCB layout

The FEE card layout avoids coupling between digital and analog signals and avoids leakage currents from high voltage sections to the extremely sensitive analog input sections (in particular because inside PHOS, humidity may be present).

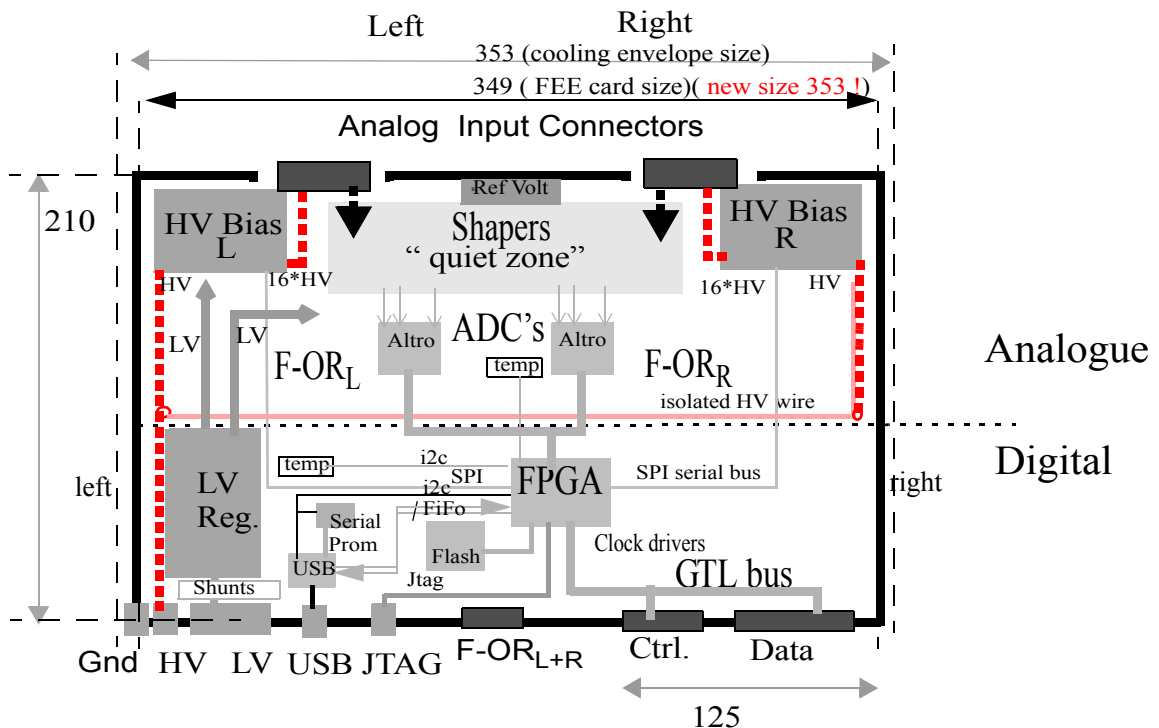


Figure 71 Regions on FEE card

Figure 71 shows the different regions on the FEE cards with its definition for LEFT and RIGHT side and quiet analogues zones, as well as digital and voltage regulator zones.

The HV zones and the left and right sides correspond to the two analogue input connectors.

The pcb layout files of the 10-layer FEE board have been produced at HUST in Wuhan under Cadence Allegro licence. The corresponding Gerber files (*.art) allow to produce PCBs or to view details of the FEE card¹.

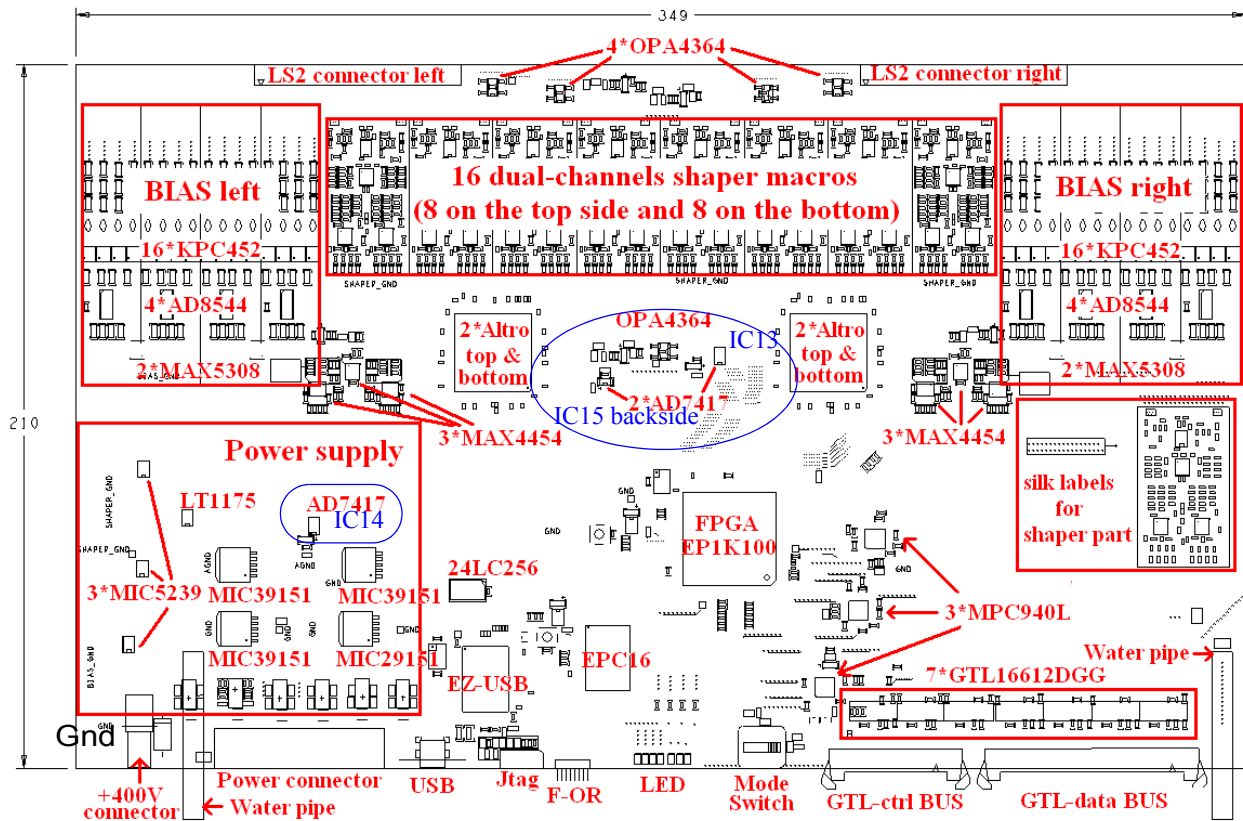


Figure 72 components areas of the FEE V 1.1a card. The position of the 3 AD7417 temperature probes is indicated in blue circles

Figure 72 depicts the main component arrangement on the FEE card version 1.1a. The shaper and Altro region is implemented in the same way on both sides of the PCB.

The position of the 3 temperature sensors IC13,14, and 15 is shown within circles.

1. A shareware viewer for Gerber files is CAM350 by D ownstream Technologies

The 10 layer stackup of FEE V1.1a is depicted in Figure 73 . It contains 4 signal layers, (TOP,L4,L7,Bottom),

COPPER	Conductor	TOP	0.017 mm
POLYIMIDE	Dielectric		0.15 mm
COPPER	Plane	L2_GND	0.035 mm
FR-4	Dielectric		0.20 mm
COPPER	Plane	L3_PWR	0.035 mm
POLYIMIDE	Dielectric		0.15 mm
COPPER	Conductor	L4	0.035 mm
FR-4	Dielectric		0.20 mm
COPPER	Plane	L5_PWR	0.035 mm
POLYIMIDE	Dielectric		0.15 mm
COPPER	Plane	L6_PWR	0.035 mm
FR-4	Dielectric		0.20 mm
COPPER	Conductor	L7	0.035 mm
POLYIMIDE	Dielectric		0.15 mm
COPPER	Plane	L8_PWR	0.035 mm
FR-4	Dielectric		0.20 mm
COPPER	Plane	L9_GND	0.035 mm
POLYIMIDE	Dielectric		0.15 mm
COPPER	Conductor	BOTTOM	0.017 mm

FEE CARD(Ver 1.1a) STACKUP

Figure 73 FEE stackup, total thickness= 2 mm

2 Ground layers (L2-GND, L9_GND) and 4 power layers (L3_PWR,L5_PWR, L6_PWR, L8_PWR).

The FEE V1.1a cards for the first PHOS module have been manufactured in FR4 material. The permission for this was granted via the agreed derogation (EDSM document 552292). CERN safety regulations (IS23) state that as from 2006, all FEE cards must be produced in halogene-free PCB materials and RoHs-compliant chip packages must be used.

Note: future FEE productions must use non-halogenated materials. In view that the dielectric constant of these material may differ from FR4, the impedances of clock and Fast OR lines must be carefully verified.

9.5 Grounding scheme

The FEE implements a very elaborate grounding scheme as depicted in Figure 74. The currents of each

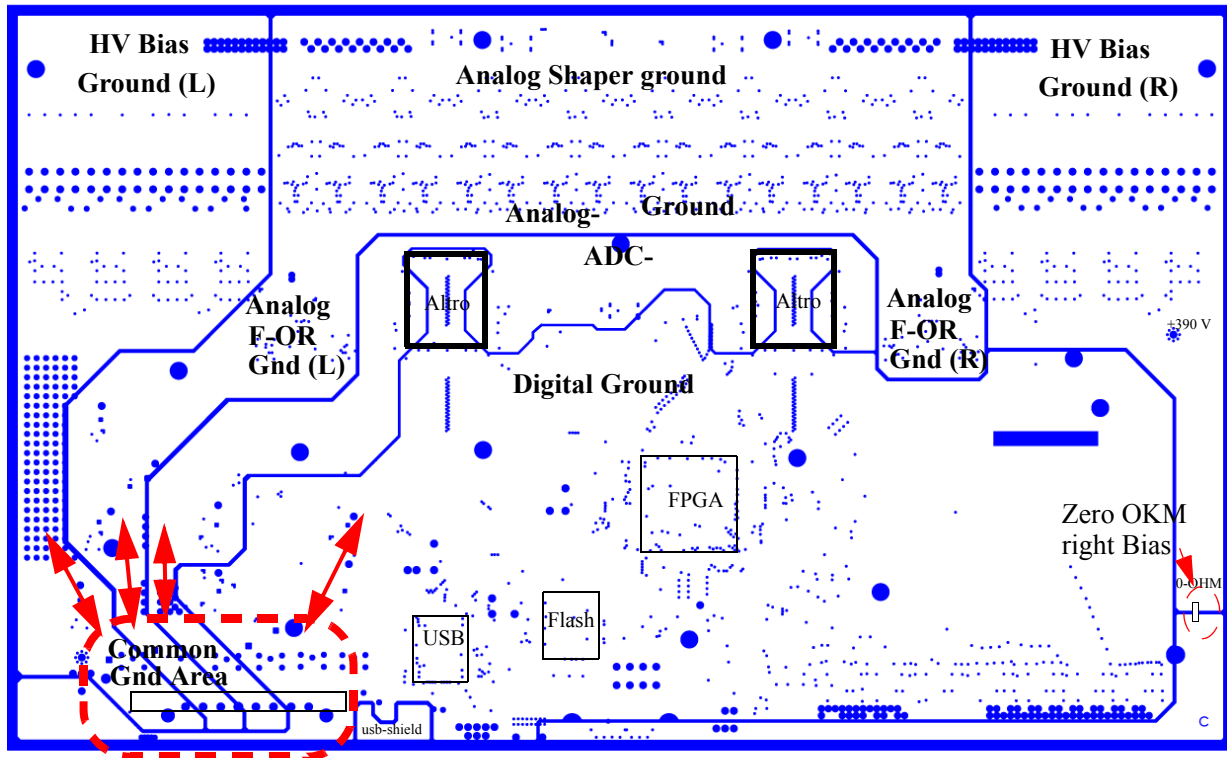


Figure 74 FEE card Rev 1.1 grounding scheme

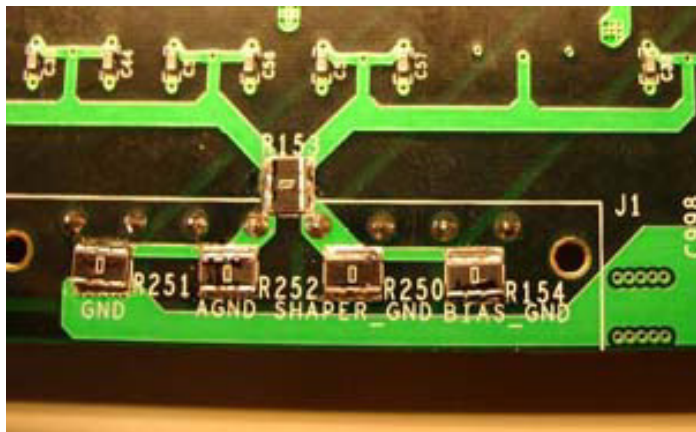


Figure 75 Ground plane equipotential zone with Zero-OHM resistors for each current line. Note that the right-side bias ground is connected via a zero ohm resistor on the right side of the FEE card.

domain ground (shaper-analog, bias-L, bias-R, ADC-analog, Digital) are routed to one single equipotential point called "common ground " close to the power connector (see Figure 75), i.e. local current fluctuations do not couple directly to other areas, the current flows back to the common ground where bulk capacitors are placed for providing the charge reserve in the low frequency range. Local charge capacitors on each ground domain such as Altro digital are dimensioned to provide enough local charge reserve in the high-frequency spectrum. If one measures the potential between shaper ground and ADC or digital ground, there may be differences up to a couple of milli-volts! For taking precise oscilloscope measurements, the oscilloscope ground reference needs to be connected to the ground which belonging of the signal of interest.

10 Triggered readout

The Alice trigger consists of level-0, level-1 and level-2 with the following latencies:

Trigger latencies (at detector):

- locally generated L1 strobe (ore'd level -0 signal from all TRU's) 650 ns.
- level-0 trigger (L1 strobe) from the TTC system is available at 1200 ns.
- level-1 trigger (L2 strobe) from TTC which closes an event in a MEB buffer 6.5 us.
- level-2 trigger which starts the readout 88 us
- level-2 messages which allow to accept/reject..... 500 us

The level-0 and level1 triggers are accept-only hardware triggers. The level-2 includes trigger messages which allow to accet or reject. Figure 76 depicts trigger sequences of events which are accepted or rejected for different

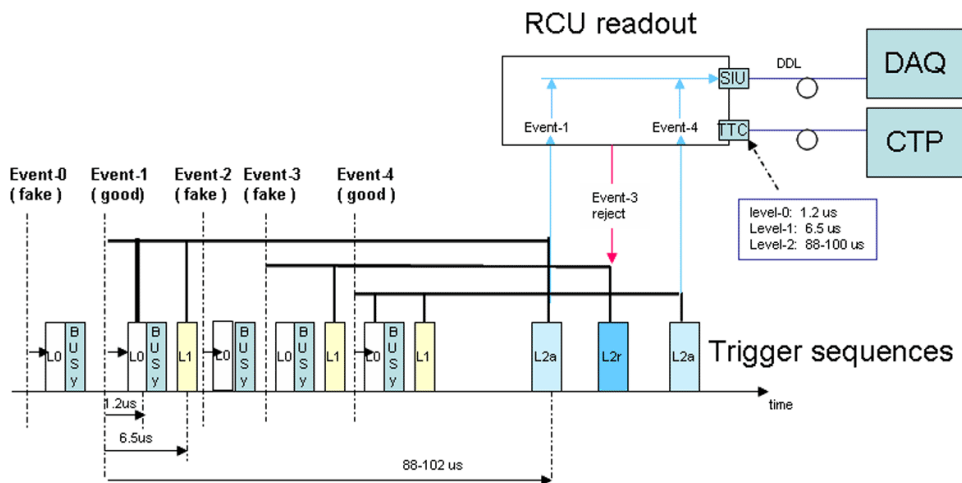


Figure 76 Trigger sequences of events

reasons.

Event -0 is fake because not confirmed by level-1

Event -1 is good because confirmed by level-1 and level-2

Event -3 is fake because of level-2 reject by the CTP level-2 reject message

Event -4 is good like Event-1

The RCU distributes both the level-0 and level-1 trigger decisions as well as the sampling clock via its two GTL bus segments A and B to the FEE cards, 28 in total.

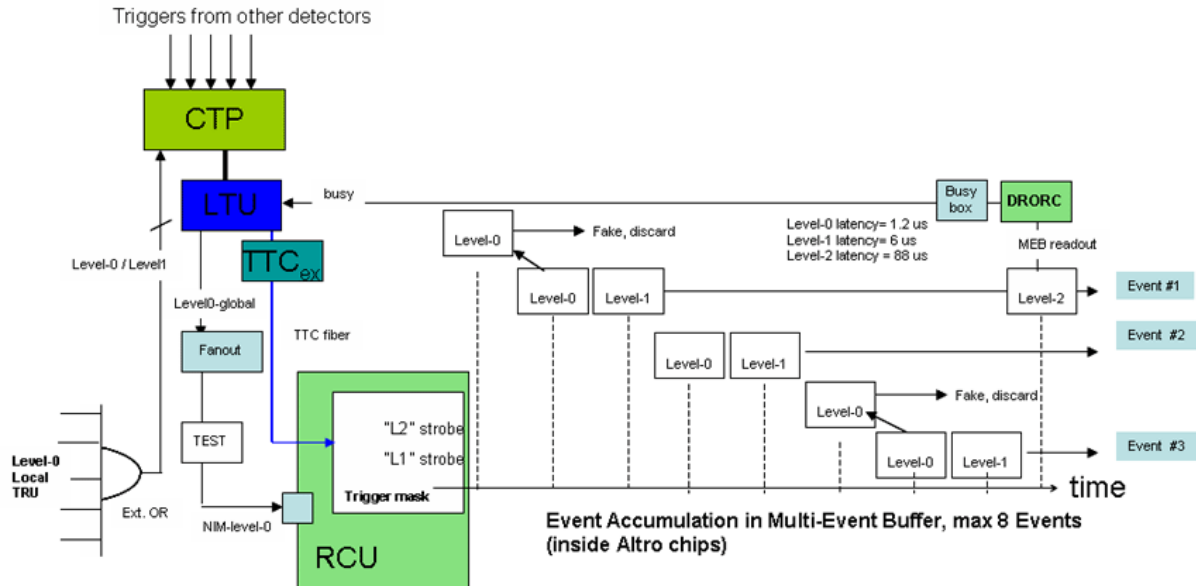


Figure 77 Trigger connectivity to RCU and event timing

The ALTRO digitizers on the FEE cards contain Multi-Event-Buffers (MEB) which are opened/closed by two timing strobe sequences (named L1 and L2) generated by the RCU as function of the level-0 and level-1 trigger. The ALTRO strobe relation with the level-x triggers is depicted in Figure 77.

Note: Other than for the TPC, the PHOS L1 corresponds to the level-0 trigger and L2 corresponds to the level-1 trigger.

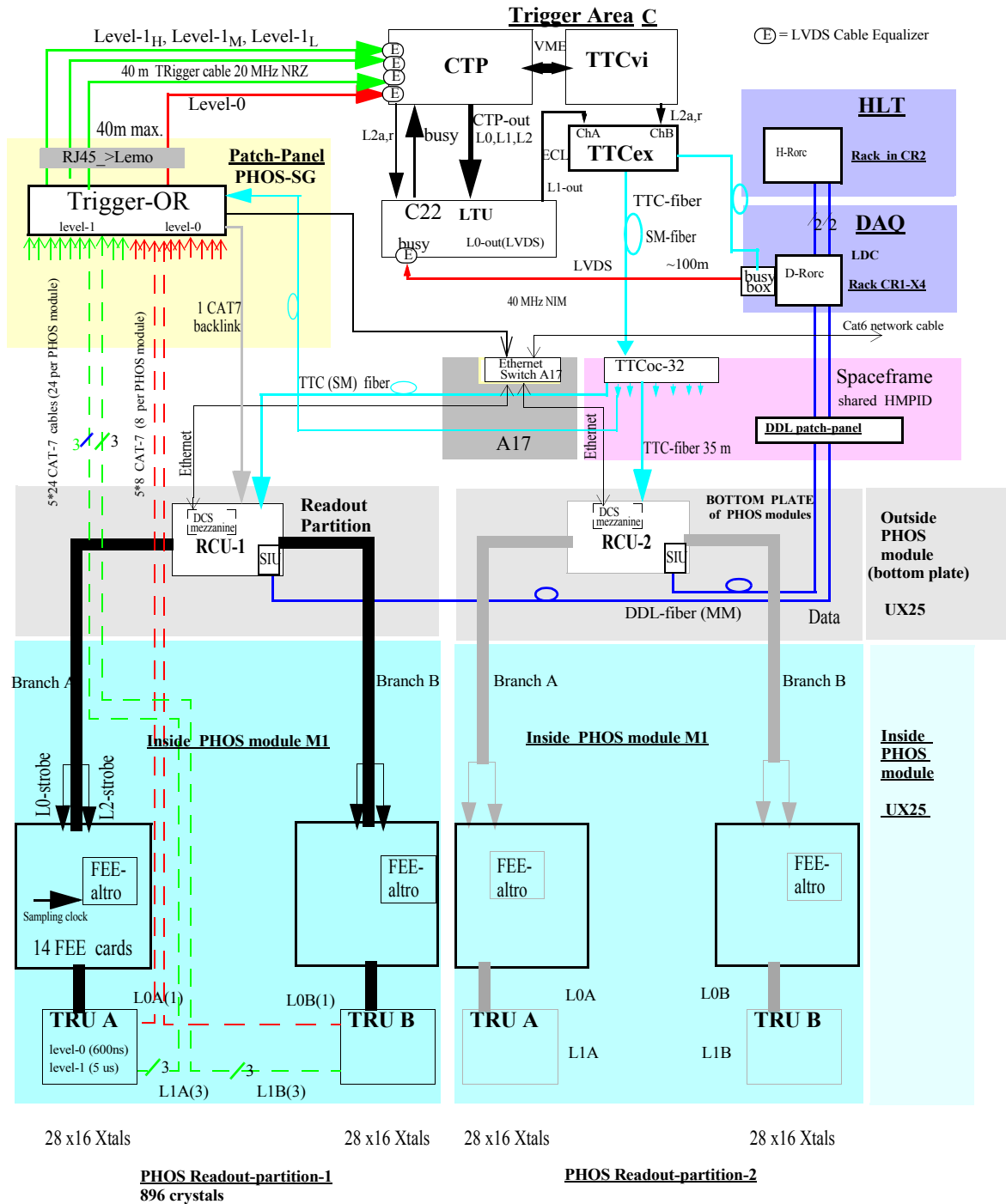
L1 opens an MEB data buffer and L2 closes it. Successive L1 signals with missing L2 strobe re-open the same buffer. L2 closes a buffer. Whenever the RCU receives a level-2 signal, it initiates the readout of the Altro buffers via its two GTL bus branches. The synchronization between level-2 triggers and their event buffers is managed by a trigger mask inside the RCU. Defacto, on each level-2 trigger, the RCU sends the CHRDO command to all Altro chips on all 14 FEE card in order to receive the data buffers which belong to the level-2 trigger.

The Altro chip has a digitization pipeline of up to 15 clocks, therefore for PHOS, the L1 strobe has a maximum latency of 1.5 us for a typical 10 MHz sampling rate.

The readout decision is taken by the RCU after a L2 trigger. Up to eight ALTRO buffers are available in the partitioned MEB buffer to be filled by L1+L2 strobe pairs with a level-2 readout. Each buffer has a maximum depth of 512 words of 10 bit. The zero-suppression feature of the Altro reduces the readout block to a minimum.

10.1 PHOS trigger connectivity overview

The connectivity for the trigger in the Alice underground area is depicted in Figure 75



11 Readout partitions and bandwidth

Four RCU partitions master the readout of all 112 FEE cards of one PHOS module (see Figure 60). The name readout partition implies that data taking with DATE can be performed for each partition independently. The full PHOS detector has consequently 20 readout partitions which are read out via DDL fibers to the DAQ and HLT computers. They are timewise synchronized by the TTC system which sends triggers and clocks to each RCU.

Each RCU consists of two branches A and B (see Figure 79). Each GTL bus branch connects 14 FEE and one TRU trigger card via a single, address mapped GTL bus. The readout of the partition is initiated when a

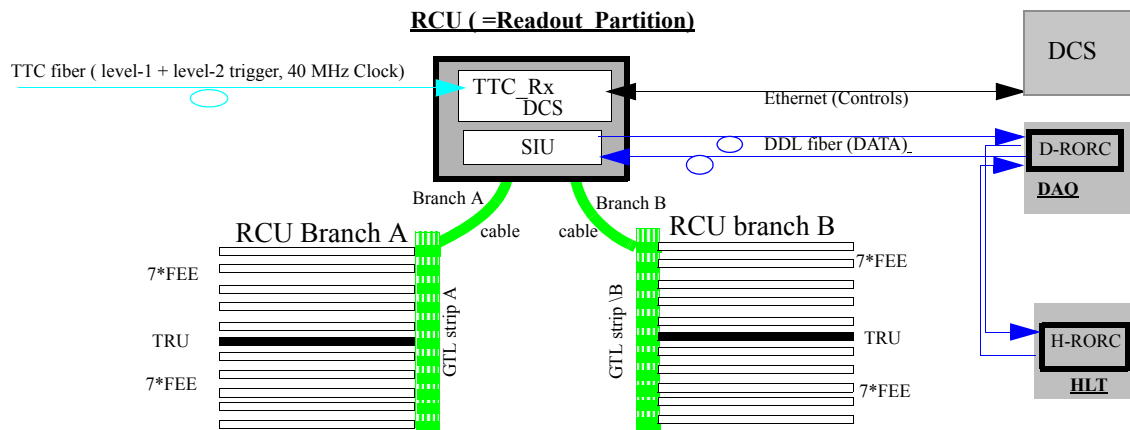


Figure 78 Connectivity of one Readout partition, consisting of 2 branches. There are 4 readout partitions per PHOS module.

level-2 trigger is received by the TTC receiver (which is physically implemented on the DCS card). The level-2 enables the readout of up to 8 events from all connected Altro Multi-Event-Buffers.

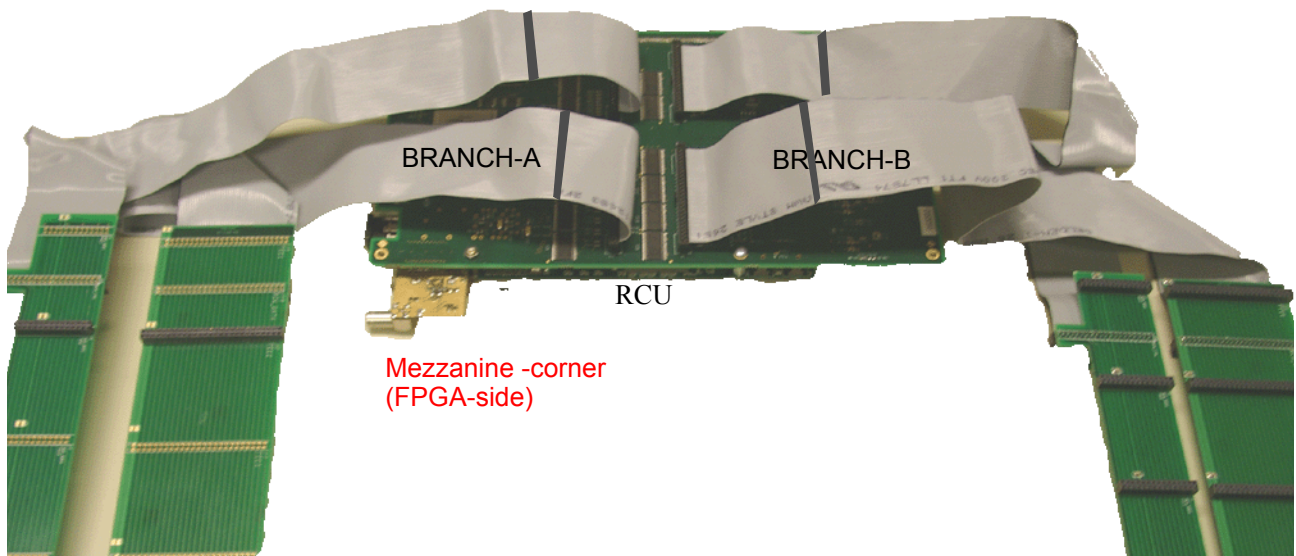


Figure 79 RCU with branch A and B cables (as seen from the bottom of the RCU)

The RCU is equipped with a DCS card [2] consisting of a networked micro-Linux subsystem which also receives via the TTL optical link the level-1 and level-2 trigger decisions, as well as the 40 MHz LHC clock.

The RCU of PHOS also contains temporarily a simple mezzanine card connector for receiving local level-0 trigger in NIM level standard for test situations (see section 27.3.1).

The sustained readout bandwidth per Readout partition is described in 11.6 .

One RCU partition is connected to 28 FEE cards with 4 Altro chips (64 readout channels) each. A "black event" consists of all recorded samples of $28 \times 4 \times 16 = 1792$ Altro buffers. A single event is framed by a level-0 and level-1 trigger strobe pair which is transmitted by the RCU and the GTL bus branches to all FEE cards.

On reception of level-2 triggers, the RCU initiates the readout by sending the Channel Redaout command (see 27.4) to all Altros. As a result, all Altros send their data blocks in sequence to the RCU. The RCU in turn combines the received event data from its two branches and sends them via the SIU and optical DDL link to the DAQ and HLT computers.

The event data of the RCU partition are transferred via the DDL link in raw data format¹ with RCU header and trailer containing N data blocks in the original Altro format. Each data block consists of m 10 bit samples and n 10 bit trailer words. On the DAQ computer, the raw data is converted in Root format and on the HLT computer the characteristic constants of the shaper pulses are extracted, thereby reducing the raw data information by a very large factor.

The Altro readout combines four 10 bit ADC's into 40 bit data words which are read out via the RCU at 40 MHz readout clock rate. The event data transmitted to the DAQ and HLT computers consist of concatenated 10 bit sample data blocks of each Altro channel, followed by two trailer words. The whole event block of one Readout Partition is framed by the RCU header / trailer. The decoder software searches for the trailer words (wordcount, hardware address) to reconstruct the individual 10 bit signal samples.

In the mode when all signal samples of all channels are read out, a very large amount of data is generated (black event mode). A significant reduction in event size is achieved by activating the the Altro zero-suppression feature (see 11.3.2) which suppresses all event samples which do not cross a user-definable signal threshold.

11.1 Readout and Trigger Configuration

There are many possible trigger and readout configurations possible via initializing specific Altro registers [17] via the DCS commands (see chapt 30).

11.1.1 Triggered readout of black events

The number of samples and presamples to be recorded per event, as well the trigger mode is defined by writing to several registers like TRCFG, DPCFB, DPCF2 (see chapter 31). The selected modes are active whenever a level-2 trigger is received. An example for enabling triggered readout of 64 fixed samples per event (black event) in test mode (trigger mode 2) is shown below:

```

w 0x7000 0x64000a      # broadcast command to Altro Trigger Config Register 0x0A
w 0x7001 0x700040      # ---> 0x40 =64 samples from L0 trigger to end
                        #....add some presamples for total No. of samples
w 0x7002 0x64000b      # broadcast to Altro Data path config register DPCFB

```

1. the Altro's zero suppression option will largely reduce the amount of the raw data volume of black events.

```

w 0x7003 0x700000      # ---> set default
w 0x7004 0x64000c      # broadcast to Altro Data path config register DPCF2
w 0x7005 0x70000F      # set number of MEB buffers to 4 and use 15 pre-samples
w 0x7006 0x390000      # close instruction memory
wait 1 us
w 0x7801 0x10bb8        # set TRCFG trigger config. register Trigger Mode =2,
                        # four buffers for the Altro MEB
                        # Tw= 0xbb8 = 3000/4 clocks between L1 and L2 = 78 us
                        # for 40 MHz readout clock
                        # now external L0 triggers can be received and
                        # Level-2 based CHRDO readout starts

w 0xF800 0x0            # only for test: receive triggers via the NIM mezzanine
w 0x0 0x0              # execute
r 0x7800               # read error status

```

After this initialization with 64 Samples and 15 pre-samples, every received L1 strobe automatically generates an L2 trigger strobe (after 78 us delay) and the RCU issues a sequence of CHRDO commands to all Altros.

Figure 212 shows the CHRDO readout sequence on the GTL bus after Level-1 and Level-2 triggers are received.

Note: in the final experiment, both the L1 and the L2 trigger must be provided by the the TTC system, hence a trigger mode 3 must be selected.

11.1.2 Zero Suppression mode

The Altro chips have a built-in zero suppression feature with several options to be defined by the user in the ZSTHR (threshold)and DPCFG (enable and mode) registers. In addition the VFPED register contains automatically calculated pedestals values and also user defined pedestals against which the raw signals can be compared.

In its simplest form, the Zero suppression circuit only records samples above a fixed programmable threshold (ZSTHR register bits <9:0>). The zero suppression feature must be enabled via bit 19 of the DPCFG register. The simplest configuration mode is a comparison against a fixed, user defined pedestal value (see Figure 81 left). This mode is chosen by selecting fpd mode via DPCFG<12:11> =0,0. In this mode, the constant pedestal value is to be stored in the register VFPED<9:0> of each single Altro channel. In the extended mode, up to 3 pre-samples below threshold can be enabled, this is to be defined in DPCFG<18:17> and the number of retained post-samples in DPCFG<16:14>. The extended mode is depicted in Figure 81, right.

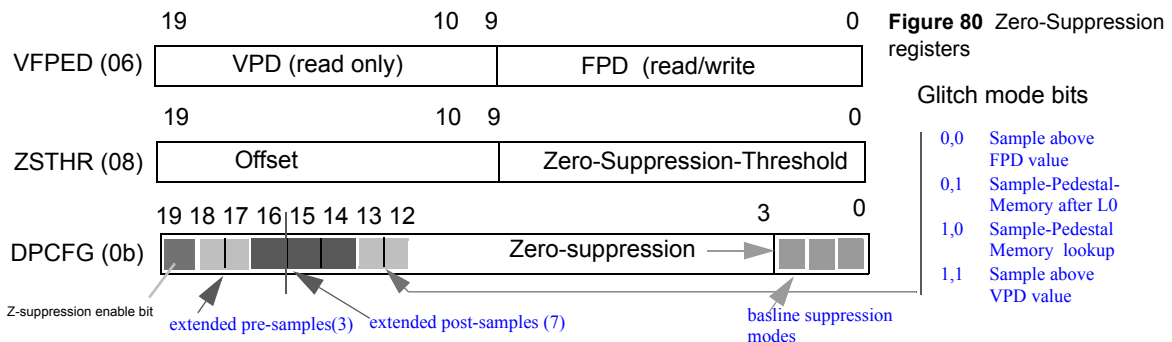


Table 4 Basline correction for Zero suppression

DPCFG[2:0]	Effect	Explanation
000	din-fpd	Sample data - global user defined value, only for tests
001	din-f(t)	Sample data - pedestal memory stored samples, starting after level-0
101	din-f(din)	
011	din-f(din-vpd)	
100	din-vpd-fpd	Sample date - selfcalibrated pedestals - global user defined value
101	din-vpd-f(t)	
110	din-vpd-f(din)	
111	f(din)-vpd-f(din-vpd)	

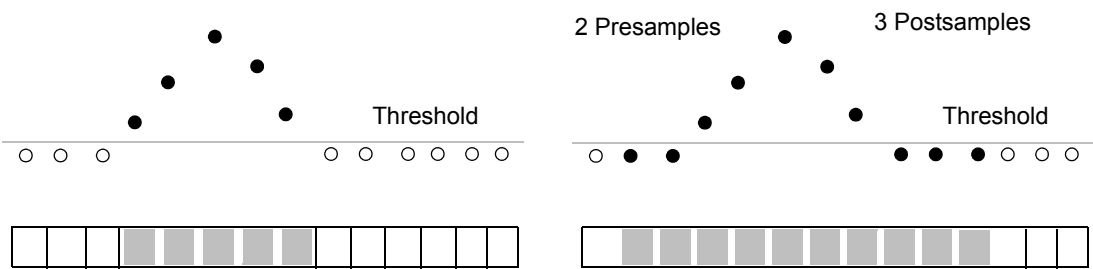


Figure 81 Zero suppression: Left basic scheme with fixed threshold. Right extended scheme with added pre and postsamples.

The following DCS scripts (for decoding see Chapter 30) are examples

a.) reading the VFPED register of some channels FEE#4 on branch A

```
w 0x7000 0x504006           # read FEE#4 branch A, Altro-0, Cannel-0, Instruction code 6
w 0x7001 0x504226           # read FEE#4 branch A, Altro-1, Cannel-1, Instruction code 6
w 0x7002 0x504446           # read FEE#4 branch A, Altro-2, Cannel-2, Instruction code 6
w 0x7003 0x39000            #xclose instruction memory
w 0x0 0x0                   # execute
wait 1us
r 0x7800                    # read error status
r 0x6000 3                  # read 3 results from result memory
```

b.) enabling triggered readout of max. 32 samples per event (zero-suppressed)

```

w 0x7000 0x64000a      # broadcast command to Altro Trigger Config Register 0x0A
w 0x7001 0x700020      # ----> 0x20 = 32 samples from L0 trigger to end
                        #....add some presamples for total No. of samples

w 0x7002 0x64000b      # broadcast to Altro Data path config register DPCFB
w 0x7003 0x7E0004      # ----> bit19=1 enable Z.S. BIT18,17=1,1 => 2 presamples retained, Mode 0x100
w 0x7004 0x64000c      # broadcast to Altro Data path config register DPCF2 @ 0xC
w 0x7005 0x700008      # set number of MEB buffers to 4 and use 8 pre-samples
w 0x7006 0x640008      # broadcast to ZSTHR register @ 0x8
w 0x7007 0x700045      # define zero-suppression threshold 0x045 ADC counts
w 0x7008 0x390000      # close instruction memory

wait 1 us

w 0x7801 0x10bb8        # set TRCFG trigger config. register Trigger Mode =2,
                        # four buffers for the Altro MEB
                        # Tw= 0xbb8 = 3000/4 clocks between L1 and L2 = 78 us
                        # for 40 MHz readout clock
                        # now external L0 triggers can be received and
                        # Level-2 based CHRDO readout starts

w 0xF800 0x0            # only for test: receive triggers via the NIM mezzanine
w 0x0 0x0               # execute
r 0x7800                # read error status

```

11.2 Raw data format

The Binary dump of one raw event (zero suppression enabled) is shown below below, obtained by the altroDump utility of David Silvermyr, ORNL

Taking max. 1 events

```
Size:2532 (header:68) Version:0x00030006 Type:PhysicsEvent
RunNb:1576
nblnRun:1 burstNb:0 nblnBurst:0 ldcld:1 gdcld:VOID
time:Fri Feb 2 15:23:57 2007
triggerPattern:00000003-00000000 detectorPattern:00000000[invalid]
- Equipment: size:2464 type:17 id:511 basicElementSize:4 attributes:
```

RCU block info:

```
BlockLength = 0x9e4
EventID1 = 0xafe
L1TriggerType = 0xe
FormatVersion = 0xa
EventID2 = 0x44
BlockAtt = 0x0
MiniEventID = 0x6
StatusAndError = 0x30
```

Data block [ADC/sample info given in hex]; N32-bit words:633 N40-bit words:480

[The formatting corresponds to four 40-bit words per full row, or 16 samples.]
Trailer blocks are used to e.g. separate the information for different channels.

trailer 0xaaa800a24f, WordCount=0, Bran=0, FECn= 4, Chip=4, Chan=15
Gain=Low

trailer 0xaaa842a24e, WordCount=66, Bran=0, FECn= 4, Chip=4,
Chan=14 Gain=High

other trailer 0xaaaa10852 (i=2); NWords=0x042 (66) TS=0x052 (82)

```
79 - 82) 0x037 0x035 0x032 0x031
75 - 78) 0x041 0x03e 0x03c 0x03a
71 - 74) 0x04d 0x049 0x046 0x044
67 - 70) 0x05b 0x057 0x054 0x050
63 - 66) 0x06c 0x067 0x063 0x05f
59 - 62) 0x07f 0x07a 0x075 0x070
55 - 58) 0x093 0x08e 0x089 0x084
51 - 54) 0x0a8 0x0a3 0x09e 0x099
47 - 50) 0x0bc 0x0b7 0x0b3 0x0ae
43 - 46) 0x0cc 0x0c9 0x0c5 0x0c1
39 - 42) 0x0d4 0x0d3 0x0d1 0x0cf
35 - 38) 0x0ce 0x0d1 0x0d4 0x0d4
31 - 34) 0x0b6 0x0be 0x0c5 0x0ca
27 - 30) 0x088 0x096 0x0a2 0x0ad
23 - 26) 0x047 0x058 0x069 0x079
19 - 22) 0x008 0x015 0x025 0x036
```

trailer 0xaaa800a24d, WordCount=0, Bran=0, FECn= 4, Chip=4, Chan=13
Gain=Low

trailer 0xaaa845a24c, WordCount=69, Bran=0, FECn= 4, Chip=4,
Chan=12 Gain=High

other trailer 0xaaaaaa845 (i=3); NWords=0x045 (69) TS=0x000 (0)

TS embedded with datawords (not in 'other trailer')...; TS=0x055 (85)

```
82 - 84) 0x034 0x033 0x030
78 - 81) 0x03d 0x03a 0x038 0x036
74 - 77) 0x046 0x044 0x041 0x03f
70 - 73) 0x052 0x04f 0x04c 0x049
66 - 69) 0x060 0x05c 0x059 0x056
62 - 65) 0x070 0x06c 0x068 0x064
58 - 61) 0x083 0x07e 0x079 0x075
54 - 57) 0x097 0x092 0x08d 0x088
50 - 53) 0x0ac 0x0a7 0x0a1 0x09c
46 - 49) 0x0bf 0x0ba 0x0b6 0x0b1
42 - 45) 0x0ce 0x0ca 0x0c7 0x0c3
38 - 41) 0x0d5 0x0d4 0x0d2 0x0d0
34 - 37) 0x0ce 0x0d1 0x0d3 0x0d4
30 - 33) 0x0b7 0x0be 0x0c5 0x0cb
26 - 29) 0x089 0x097 0x0a3 0x0ad
22 - 25) 0x04b 0x05c 0x06c 0x07b
18 - 21) 0x00f 0x01b 0x02a 0x03a
```

trailer 0xaaa800a24b, WordCount=0, Bran=0, FECn= 4, Chip=4, Chan=11
Gain=Low

trailer 0xaaa842a24a, WordCount=66, Bran=0, FECn= 4, Chip=4,
Chan=10 Gain=High

other trailer 0xaaaa10852 (i=2); NWords=0x042 (66) TS=0x052 (82)

```
79 - 82) 0x038 0x035 0x033 0x031
75 - 78) 0x042 0x03f 0x03d 0x03a
71 - 74) 0x04e 0x04b 0x048 0x045
67 - 70) 0x05c 0x059 0x055 0x052
63 - 66) 0x06d 0x069 0x064 0x060
59 - 62) 0x080 0x07b 0x076 0x071
55 - 58) 0x094 0x08f 0x08a 0x084
51 - 54) 0x0a9 0x0a4 0x09f 0x099
47 - 50) 0x0bc 0x0b8 0x0b3 0x0ae
43 - 46) 0x0cc 0x0c9 0x0c5 0x0c1
39 - 42) 0x0d4 0x0d3 0x0d1 0x0cf
35 - 38) 0x0ce 0x0d1 0x0d3 0x0d4
31 - 34) 0x0b6 0x0bf 0x0c5 0x0ca
27 - 30) 0x089 0x097 0x0a2 0x0ad
23 - 26) 0x048 0x05a 0x06a 0x07a
19 - 22) 0x009 0x016 0x026 0x037
```

trailer 0xaaa800a249, WordCount=0, Bran=0, FECn= 4, Chip=4, Chan= 9
Gain=Low

trailer 0xaaa844a248, WordCount=68, Bran=0, FECn= 4, Chip=4, Chan= 8
Gain=High

last sample(s): 83 - 84) 0x031 0x033

other trailer 0x110540c433 (i=0); NWords=0x044 (68) TS=0x054 (84)

```
79 - 82) 0x03b 0x039 0x037 0x035
75 - 78) 0x045 0x042 0x040 0x03d
71 - 74) 0x050 0x04e 0x04a 0x048
67 - 70) 0x05f 0x05b 0x057 0x054
63 - 66) 0x06f 0x06b 0x067 0x063
59 - 62) 0x082 0x07d 0x079 0x074
55 - 58) 0x096 0x091 0x08c 0x087
51 - 54) 0x0ab 0x0a6 0x0a1 0x09c
47 - 50) 0x0bf 0x0bb 0x0b6 0x0b0
43 - 46) 0x0cf 0x0cb 0x0c7 0x0c3
39 - 42) 0x0d7 0x0d6 0x0d4 0x0d2
35 - 38) 0x0d1 0x0d5 0x0d6 0x0d7
31 - 34) 0x0ba 0x0c2 0x0c8 0x0cd
27 - 30) 0x08c 0x09a 0x0a7 0x0b1
23 - 26) 0x04c 0x05d 0x06e 0x07e
19 - 22) 0x00e 0x01b 0x02a 0x03b
```

trailer 0xaaa842a247, WordCount=66, Bran=0, FECn= 4, Chip=4, Chan= 7
Gain=High

other trailer 0xaaaa10852 (i=2); NWords=0x042 (66) TS=0x052 (82)

```
79 - 82) 0x037 0x035 0x033 0x031
75 - 78) 0x041 0x03f 0x03c 0x039
71 - 74) 0x04d 0x04a 0x047 0x044
67 - 70) 0x05b 0x057 0x054 0x051
63 - 66) 0x06c 0x068 0x063 0x05f
59 - 62) 0x07e 0x07a 0x075 0x071
55 - 58) 0x092 0x08d 0x088 0x083
51 - 54) 0x0a7 0x0a2 0x09d 0x098
47 - 50) 0x0ba 0x0b6 0x0b1 0x0ac
43 - 46) 0x0c9 0x0c6 0x0c3 0x0be
39 - 42) 0x0d0 0x0cf 0x0ce 0x0cc
35 - 38) 0x0cb 0x0ce 0x0d0 0x0d0
31 - 34) 0x0b3 0x0bb 0x0c2 0x0c7
27 - 30) 0x087 0x094 0x0a0 0x0aa
23 - 26) 0x047 0x058 0x068 0x078
19 - 22) 0x00a 0x016 0x026 0x036
```

etc....

The decoding of the raw data is following a back-linked list according to the Altro Data block format [17] depicted in Figure 82.

The full data block at the Computer consists of an 68 byte RCU header, which is followed by raw data blocks

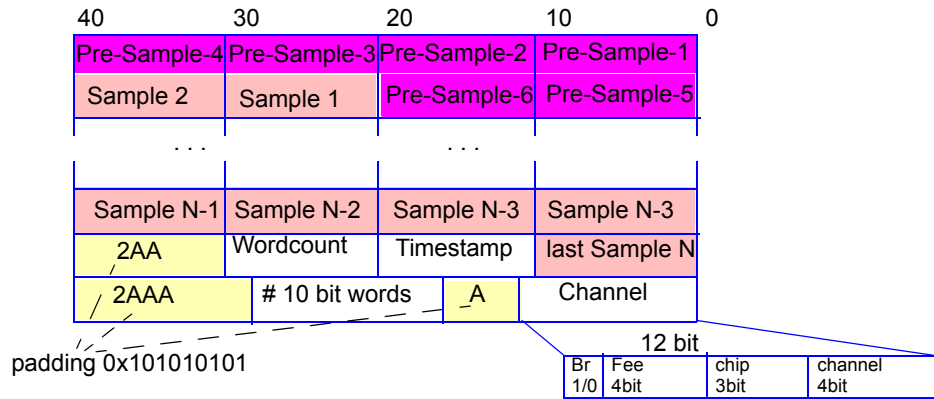


Figure 82 Altro back-linked Data Block

of consecutive 10 bit Altro samples which are formatted in 40 bit words. Each Altro block represents the consecutive samples taken by one Altro channel, followed by two 40 bit trailers. The trailers contain the 12 bit full address of the corresponding channel, a 10 bit wordcount and timestamp. Due to the variable choice of samples, in particular with varying sample sizes after zero-suppression, padding fillers are added to the two trailer words.

11.3 Event size and bandwidth

Black event mode is very useful for commissioning. All PHOS channels are read out whenever a readout trigger is received. Zero suppressed mode compresses the offline data volume according to the occupancy of the physics runs. Other possibilities to reduce the amount of data are by the HLT computers and by reducing the number of samples and sampling frequency to a minimum.

11.3.1 Black event mode

The event size per RCU partition for “black events” is simply the number of channels per partition (for PHOS $N_c = 2 * 896$) multiplied by the Number of bits per sample, multiplied by the number of samples N_s plus some header/trailer overhead (8 byte) per channel..

$$\text{Size}_{\text{blackevent}} = 10/8 \times (N_s + 8) \times 1792 [\text{byte}]$$

$$\text{SIZE}_{\text{black, 1 partition (Ns=32)}} = 89.6 \text{ kbyte}$$

$$\text{SIZE}_{\text{black, 1 partition (Ns=64)}} = 179.2 \text{ kbyte}$$

$$\text{SIZE}_{\text{black, 1 PHOS (Ns=32)}} = 358 \text{ kbyte}$$

$$\text{SIZE}_{\text{black, 1 PHOS (Ns=64)}} = 716.8 \text{ kbyte}$$

The readout bandwidth is the Event-size multiplied by the level-2 trigger rate

100 Hz max level-2 trigger rate:

$$\text{BW}_{\text{black,1 PHOS (Ns=32), (100 Hz)}} = 31.5 \text{ Mbyte/s}$$

$$\text{BW}_{\text{black,1 PHOS (Ns=64), (100 Hz)}} = 63 \text{ Mbyte/s}$$

11.3.2 Zero-Suppressed mode

As seen in the previous chapter, the readout bandwidth produced by the black event mode must be reduced significantly in order to allow PHOS to run at trigger rates of 1 kHz.

The zero suppression option of the Altro chips collapses the raw data output from each Altro since only samples above the pedestal threshold are transmitted. Hence, depending on the detector occupancy, only samples from channels with signals above threshold are transmitted.

A.) proton-proton physics

With an estimated occupancy in the order of 1% and 1kHz level-2 trigger rate:

$$\text{BW}_{\text{Zero-S,P-P, PHOS (Ns=32), (1 kHz)}} = 0.35 \text{ Mbyte/s}$$

$$\text{BW}_{\text{Zero-S,P-P,PHOS (Ns=64), (1kHz)}} = 0.71 \text{ Mbyte/s}$$

B.) Heavy Ion Physics

the minimum bias trigger occupancy is 10- 40%

$$\text{BW}_{\text{Zero-S, HI 40%, PHOS (Ns=32)}} = 143 \text{ Mbyte/s}$$

$$\text{BW}_{\text{Zero-S, HI 40%, PHOS (Ns=64)}} = 286 \text{ Mbyte/s}$$

The readout bandwidth of 286 Mbyte/s for Heavy Ion runs is technically sound with 4 DDL links however from the point of view of offline data volume, it is still too much.

For this reason, the HLT computers, which receive the PHOs raw data, will reduce this data volume consisting originally of $N \times 20$ bit ADC samples per event by realtime conversion (1 kHz = 1 m conversion time) of signal samples into the following physics characteristics of the signal shape:

- peak signal amplitude (= Energy [see 8.4])
- pedestal (= reference & noise level , [see 4])
- Time of flight (time at first or second derivative point of Gamma-2 pulse fit) [see 5.1]

11.4 Number of Samples

Based on a PHOS shaping time of 1 μ s, in order to reconstruct the signal and apply the best fit, the minimum number of samples are defined by the Nyquist theorem that the sampling frequency should be $>$ the bandwidth of the shaper signal which is 500 kHz for the PHOS shaper. Hence the minimum sampling rate is 1 MHz.

11.5 Max trigger Rate

Due to a clear limitation of the effective DDL link bandwidth around 100 Mbyte/s the maximum trigger rate is

$$\text{Max Trigger rate} < 100 \text{ Mbyte/s (DDL limit)} / \text{Event size}$$

This relation is shown for black event in Figure 83 which indicates that the number of samples (assuming only

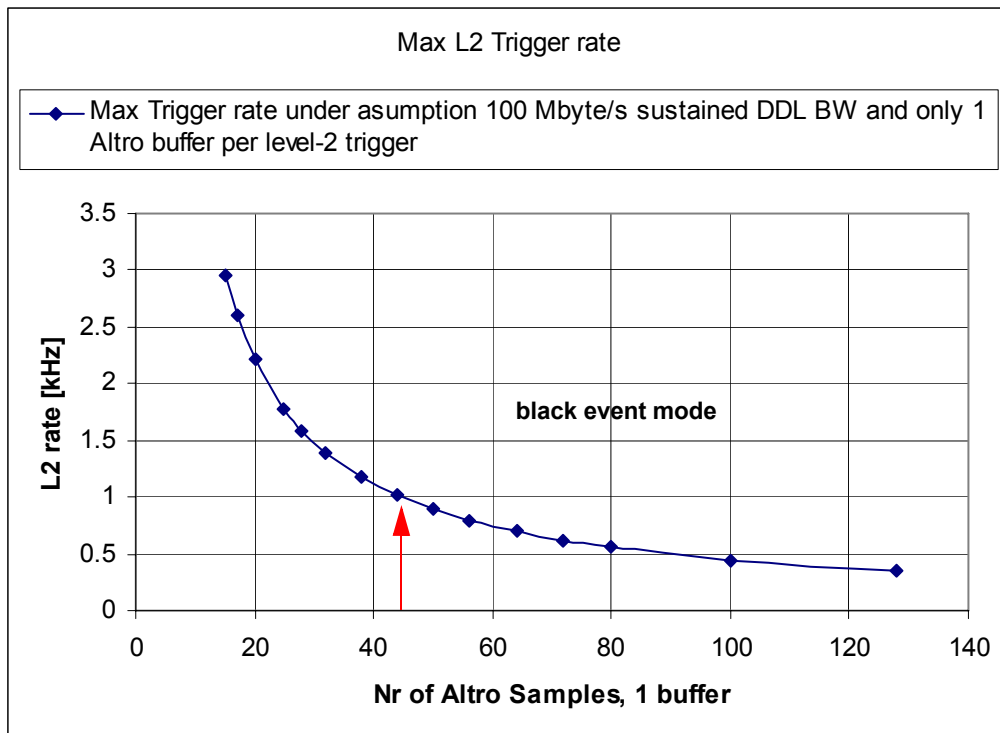


Figure 83 Readout limit of Level-2 rate versus number of Altro samples

1 event buffer on average per level-2 trigger) should be less than 45 in order to allow level-2 rates of 1 kHz. With 32 samples and 8 words overhead this condition is met.

For zero-suppressed mode, the occupancy figures for p-p (1%) and for lead-lead (10-40%) can be used to scale the black event mode to higher level-2 rates.

11.6 Readout Bandwidth

The maximum readout bandwidth per RCU branch is defined by the bandwidth at which each all Altros of the partition send data to the RCU and by the overhead which the RCU needs in order to master the Altro readout list.

Whenever a Level-2 trigger is received by the RCU, it issues the CHRDO macro which initiates in sequence all Altros contained in RDO list (see chapt 14.1) to send their data buffers to the RCU. This results in a sequence of block transfers¹ until all Altros in the RDO list have sent their event data to the RCU.

The intrinsic Altro bandwidth is 40 MHz @ 40bit = 200 Mbyte/s. As seen in Figure 211: the deadtime overhead between individual ALTRO data blocks is ca 0.65 us. This corresponds to 25 readout samples at 40 MHz. Hence the effective bandwidth Altro bus bandwidth during CHRDO transfers can be expressed as function of the blocksize (Samples +8 headers) as follows:

$$BW[Mbyte/s] = 200 \cdot \left(1 - \frac{1}{1 + Blocksize/25}\right)$$

1. block transfers means transfers which are strobed by the TRSF signal

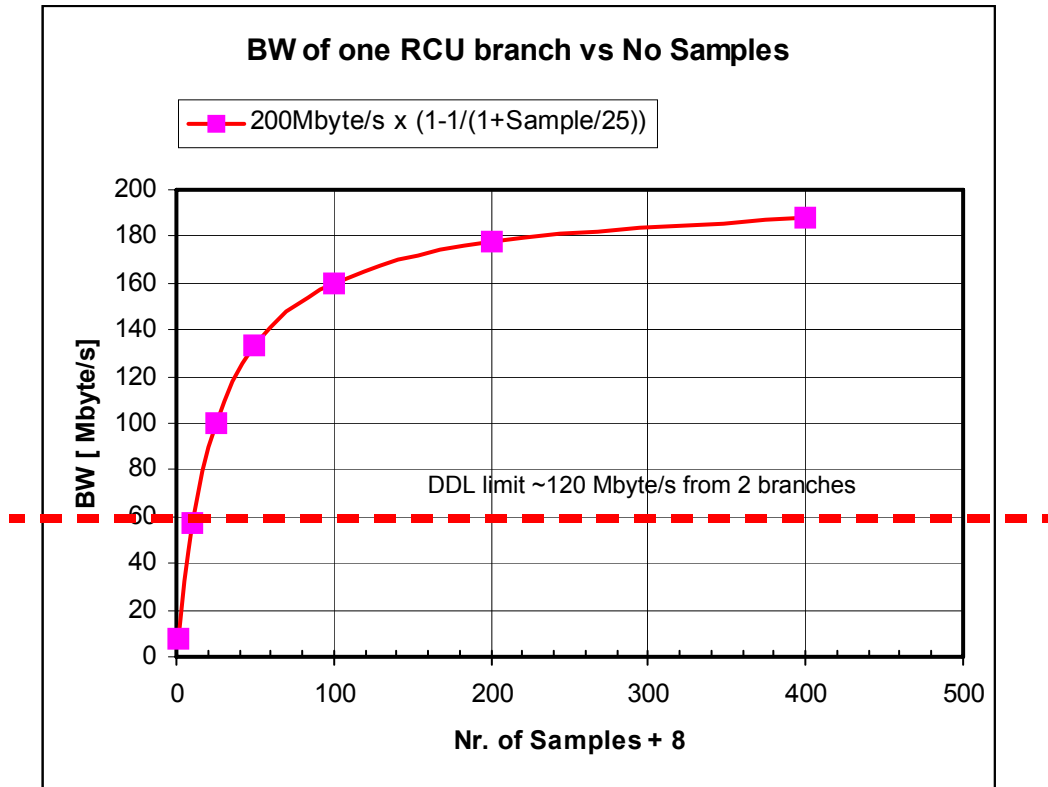


Figure 84 Bandwidth of one RCU branch as function of blocksize (Nr. of samples+8)

For small CHRDO readout blocks of 32 samples and 8 word overhead (blocksize 40) the effective readout bandwidth is 60% of the maximum bandwidth of large event sizes which approaches asymptotically 200 Mbyte/s)

Since the RCU reads out two branches in parallel and since the upper limit of the DDL link is in the order of 120 Mbyte/s the local bandwidth of individual RCU branches shown in Figure 84 is defacto limited at the output to the DDL link to 120 Mbyte/s as the integral value.

Hence for black event mode and assuming a sample size of 32, hence $\text{SIZE}_{\text{black, 1 partition (Ns=32)}} = 89.6 \text{ Mbyte}$

the maximum allowed level-2 trigger rate is 1 .. 2 Hz !

12 GTL backplane

In order to use the RCU and related software and firmware environment that exists for the TPC, PHOS has adopted the GTLbackplane bus and readout backend concept from the Alice TPC, with several modifications.

The switching levels of the GTL+ bus standard are depicted in Figure 85 below. The Reference Voltage (1 Volt

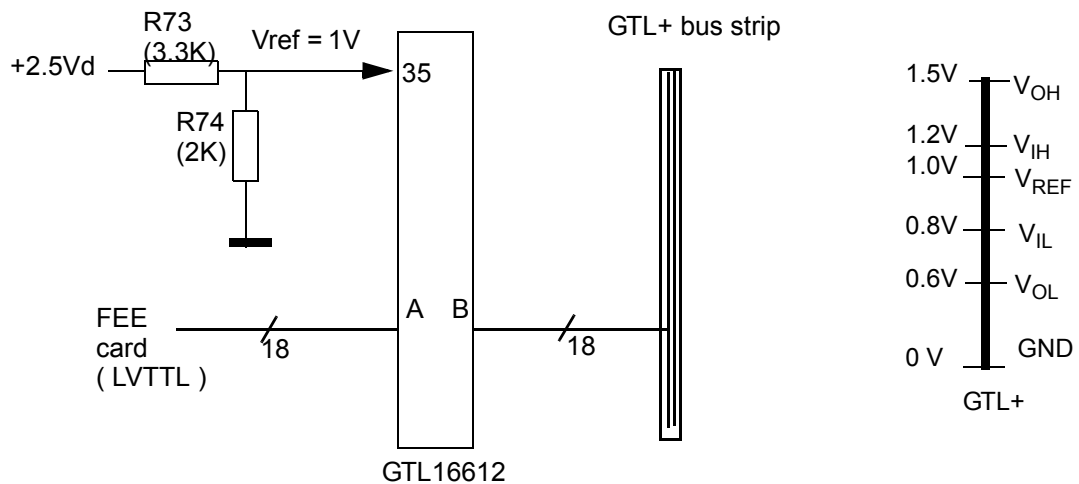


Figure 85 GTL+ bus switching levels

nominal) for incoming signals on the FEE is defined by two voltage divider resistors on the FEE card¹.

The PHOS-internal GTL bus branches of Figure 60 are connected via 40 cm branch cables of 75 OHM impedance to the RCUs which are mounted outside the PHOS embedded volume. Figure 60 shows the 8 GTL bus branches of one PHOS module with branch cables for connection to the RCU. Since every RCU masters 2 branches, there are 4 RCU partitions, each consisting of 28 FEE cards (896 crystals). The FEE slot spacing of one branch is 45.4 mm, allowing for 14 FEE cards and one TRU in the middle of the bus at address 0

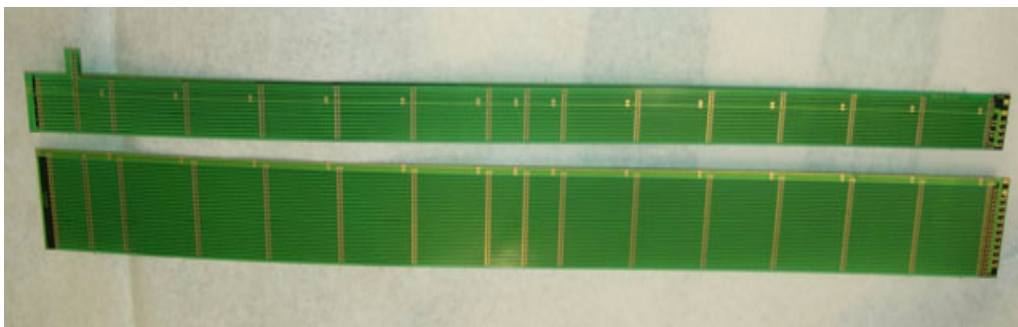


Figure 86 GTL bus strips, top: control bus, bottom: data bus. The termination resistor network is on the right side, the cable connection on the left side. The TRU slot is in the middle between two FEE connectors

The PHOS GTL bus consists of a control and a 40 bit data bus with 14 FEE positions (Figure 86)

1. incoming signals on the RCU are equally referenced

The overview over the RCU-FEE bus concept is depicted in Figure 91. The GTL bus for 40 bit data and the

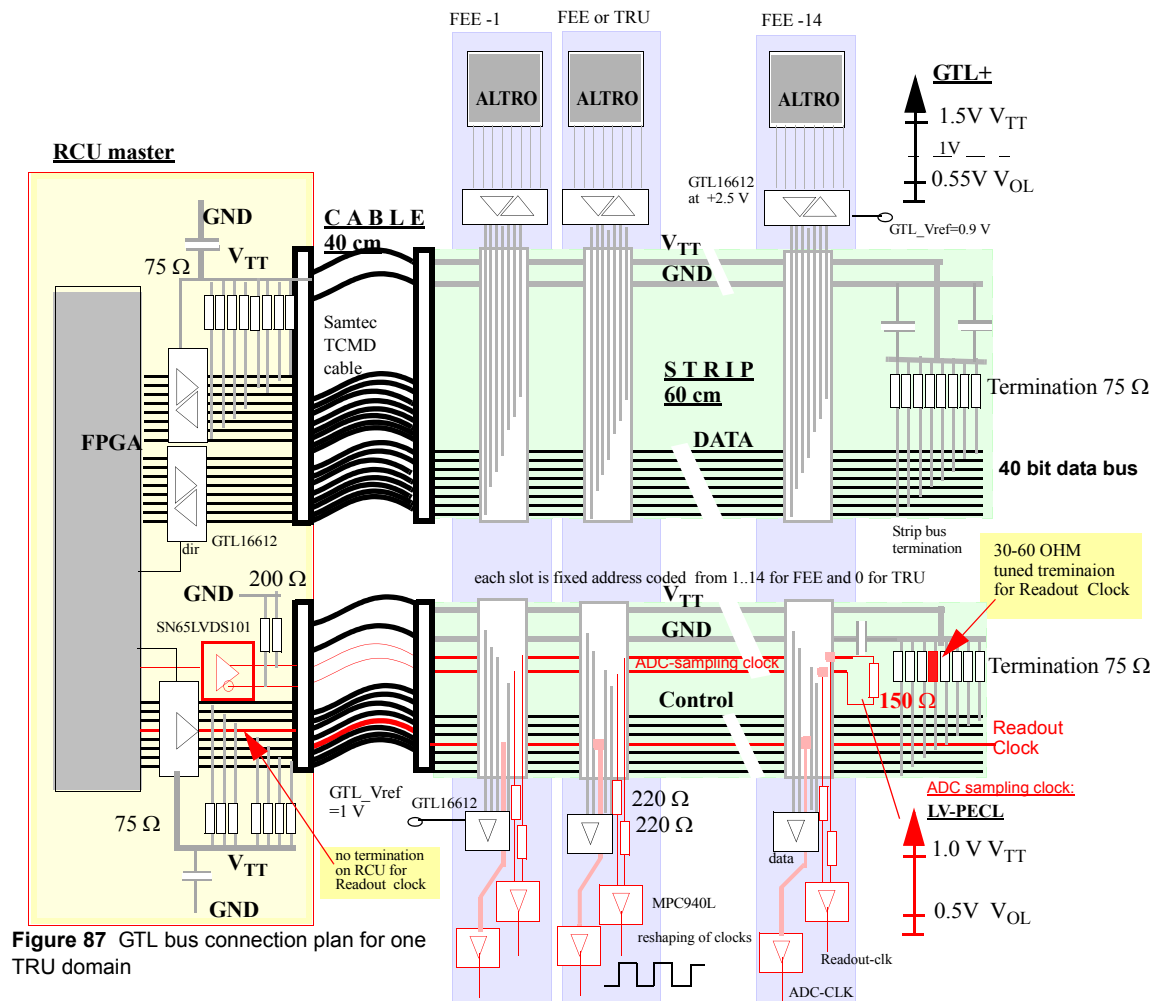
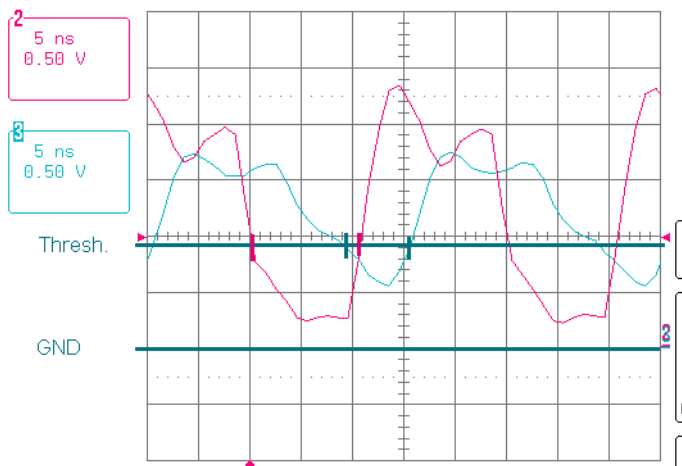


Figure 87 GTL bus connection plan for one TRU domain

control bus is connected between GTL drivers of type GTL16612 on both RCU and FEE cards. There are 14 FEE and 1 TRU connector per GTL backplane spaced by 45.4 mm, the capacitive load per FEE card is ca. 6 pF.

The unloaded bus impedance of 75 OHM drops under full load to 30 OHM. Hence it is important that the crucial 40 MHz readout clock which is driven by the RCU, is terminated at the end of the GTL bus by a tuned termination resistor according to the real multi-load situation (between 30..60 OHM).

The 40 MHz readout clock measured on the GTL bus is shown in Figure 88. This clock is driven by the RCU and terminated at the end of the GTL bus with R6 which has to be tuned with data between 30 and 60 OHM. With a 1 Volt GTL threshold, both Slot #1 and Slot #14 see the clock and an MPS 940 clock chip regenerate a symmetrical waveform on the FEE cards.



Note: the clock signal delay between FEE1 and FEE14 is 5ns and the amplitude at FEE slot #14 is significantly attenuated. The threshold for the GTL receivers is 1 Volt (defined by R73 and R74 on the FEE card). By changing the termination resistor R6 for the Readout clock on the GTL control bus, the position of the RCLK signal relative to the threshold can be changed.

Figure 88 Readout Clock on GTL bus: red on FEE #1, blue on FEE #14.

The DSTB strobe of the Alto data CHRDO readout protocol has inverse direction, meaning that it is generated on the FEE cards and terminated at the RCU side.

In case of readout errors the GTL threshold on the RCU is defined by R93 on the RCU. The RCU threshold is by default 940 mV with R93 = 950 OHM. It can be reduced to 620 OHM for a threshold of 680 mV

Figure 89 shows the installation of the GTL bus to groups of 14 FEE cards.

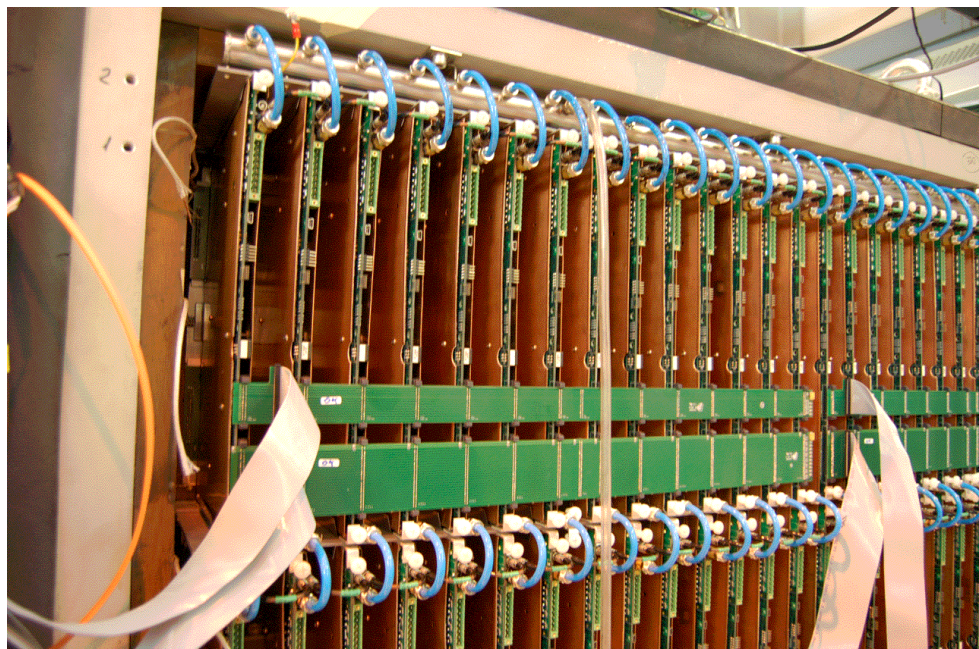


Figure 89 GTL bus installed on FEE cards backside inside PHOS module.

The GTL bus itself is a FR4 stackup of 0.680 mm total PCB thickness [Figure 90] the bussed signal transmission

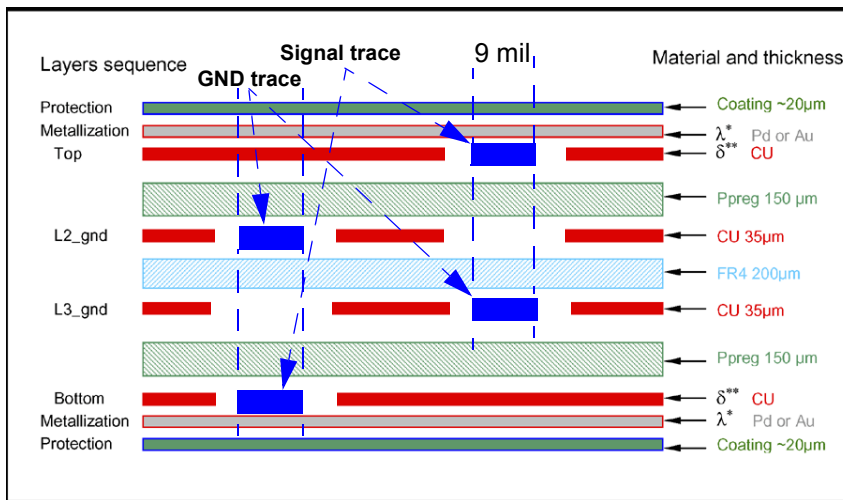


Figure 90 Stackup of GTL strip backplane: Class-4 PCB, 4 conductive layers, total thickness 678 µm, $1\mu\text{m} < \lambda < 3\mu\text{m}$, $\lambda + \delta \sim 35\mu\text{m}$

lines are 9 mil wide, parallel traces of 35 µm copper, separated by two dielectric layers. Due to the embedded

GTL control

GTL-Data

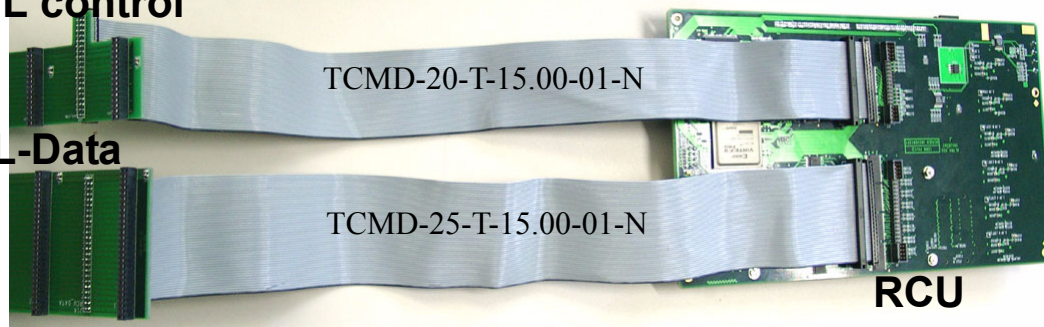


Figure 91 GTL branch A, connected on backside of RCU-4 as for testcrate

mounting of FEE cards inside a closed volume, the GTL bus has to be extended via cables to the externally situated RCU.

Figure 91 shows the details of this connection for RCU branch A. The Samtec TCMD cable have a length of 15 inch (=38.1 cm) and must have connectors of opposite polarity on both ends. The connector with pins are to be soldered to the GTL strips as shown. The plugs are inserted to the RCU branch connectors. The shown branch corresponds to RCU branch A. The connection to Branch B requires that the connectors are plugged in the same orientation as branch A, only displaced to the right side branch B connectors (i.e. do not rotate by 180 degree).

The correct connection of branch A and B for mounting inside PHOS is shown in Figure 79.

Note: Branch A is the branch connector on the side of the DDL link optical connector

The address decoding on PHOS GTL bus starts (different from TPC !) at address 1 and ends at address 14. The TRU trigger card is placed at address #0 in the centre of the GTL strips. The geographical address scheme for PHOS is depicted in Figure 92. It shows also one particularity of PHOS that the 4 Altro chips within each FEE card are implemented at non-contiguous hardware addresses.

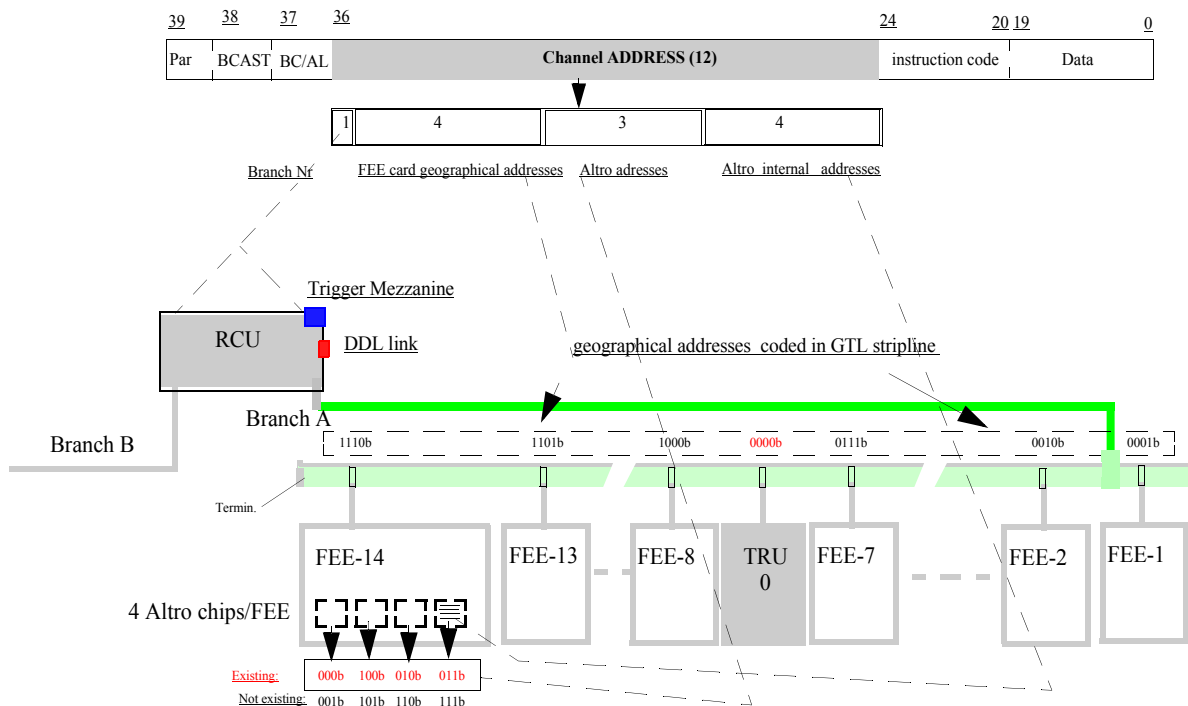


Figure 92 Geographical address mapping of PHOS for FEE and Altro chips. The first FEE card (closest to RCU) is at channel address 0x1. The central TRU trigger card is at address 0x0.

13 FEE Power supply and control

The FEE Power connections and nominal currents are shown in Figure 93 relative to the FEE power connector.

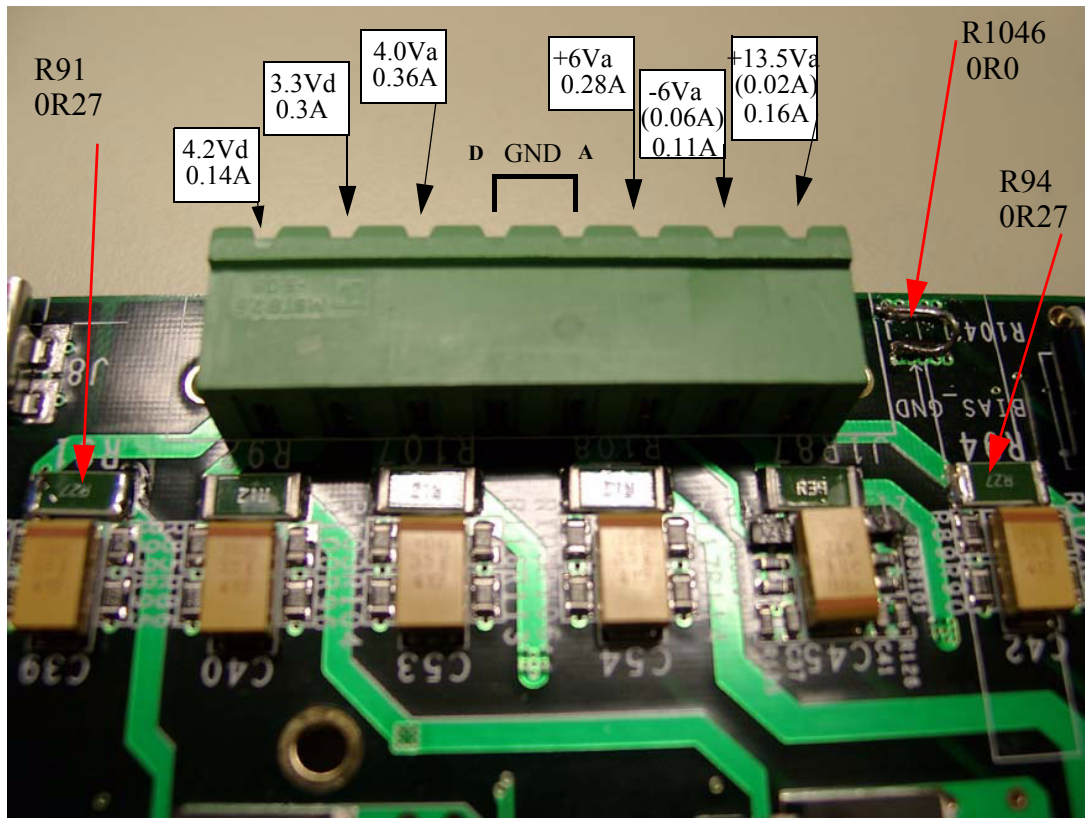


Figure 93 Power connections and currents of FEE V1.1

A basic test is to measure the voltages at the connector as shown.

Note: LV should not be applied without GTL bus and RCU connected and initialized. The +13 volts are in practise delivered by a separate power supply than the other voltages. Apply first the other voltages and then +13 Volt.

Before taking data with an RCU, initialization and configuration script have to be run. In laboratory situations this is to be done via the rcu shell scripts like init.scr on the DCS Linux card. The DCS is the software master of the RCU. For manual debugging, push the Reset button on the FEE card. The real Voltages and currents corresponding to Figure 93 can be read via their corresponding PCM registers (see 13.3.4).

The PCM firmware sets the bias voltages to a default reset value (typically 245 Volt). The minimal Voltage is ca 210 Volt. In laboratory situations,DCS scripts like described in chapter 15 are to be used to change the bias Voltages. In the experiment APD bias control is available via user interface software communicating with the DCS card via an fee server.

Note: Bias Voltages below 210 Volt can be produced by reducing the input Voltage below this value.

Note: Always disable triggers before running DCS scripts. Triggers must only be applied during runs.

As shown in Figure 94 the LV power supply is provided by 8 color-coded cables of 2.5 mm² copper diameter

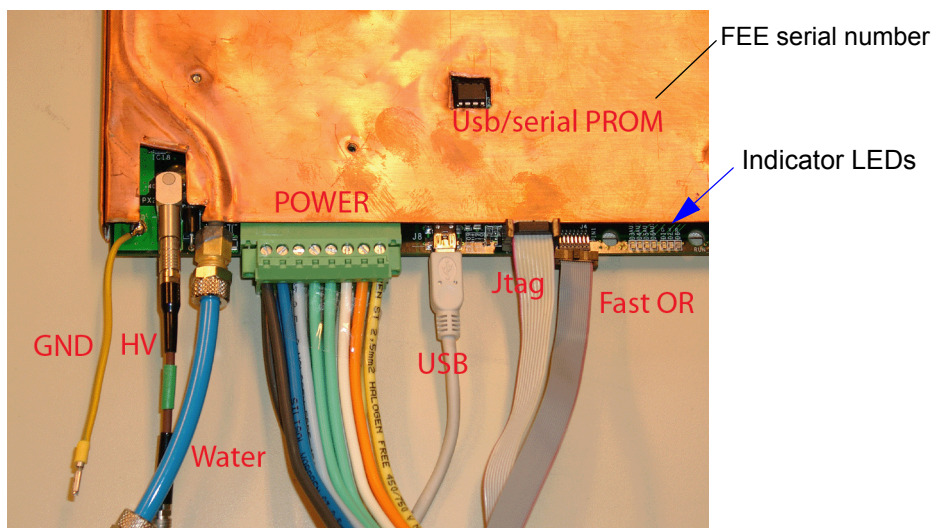


Figure 94 FEE connections of FEE card mounted inside the water-cooling cassette.

which is daisy chained between FEE cards (see Figure 96). The cable connector (Phoenix **MSTB 2,5/8-GF-5,08**) is fixed by screws to the FEE cards. Power supplies with both current and voltage displays are preferable for laboratory situations since the current display can give information about proper operation. Figure 95 depicts details of daisy-chained LV power cable Using 2.5 mm² cables the maximum voltage drop between the 1st

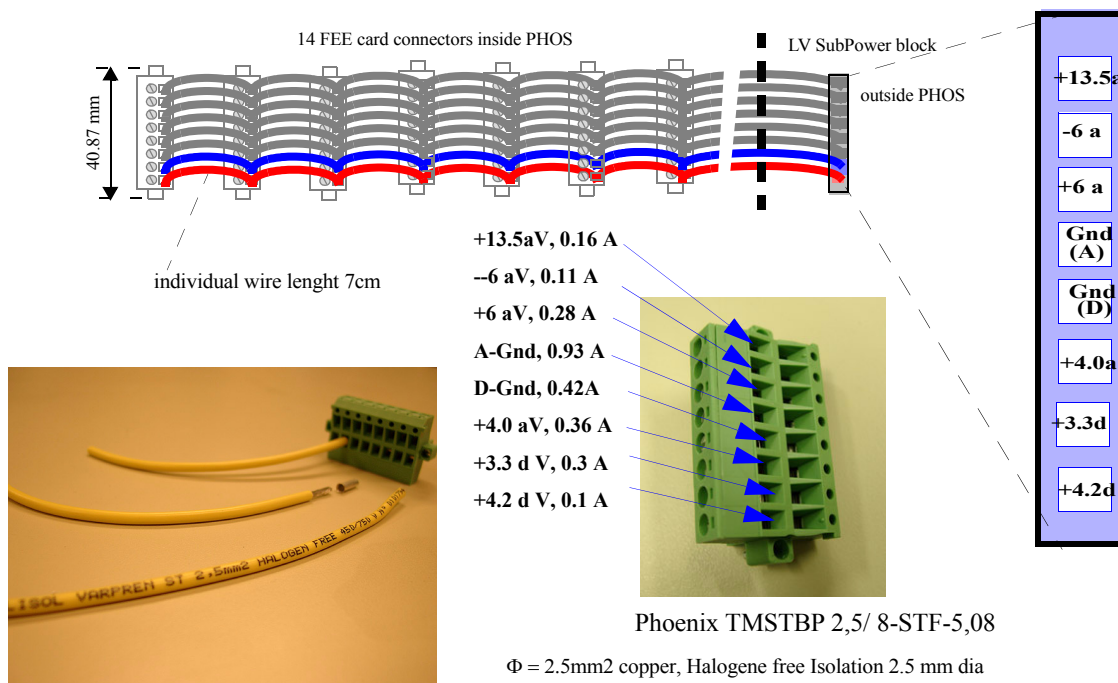


Figure 95 daisy-chained LV power bus for FEE cards

and the 14th FEE card was measured 30 mV.

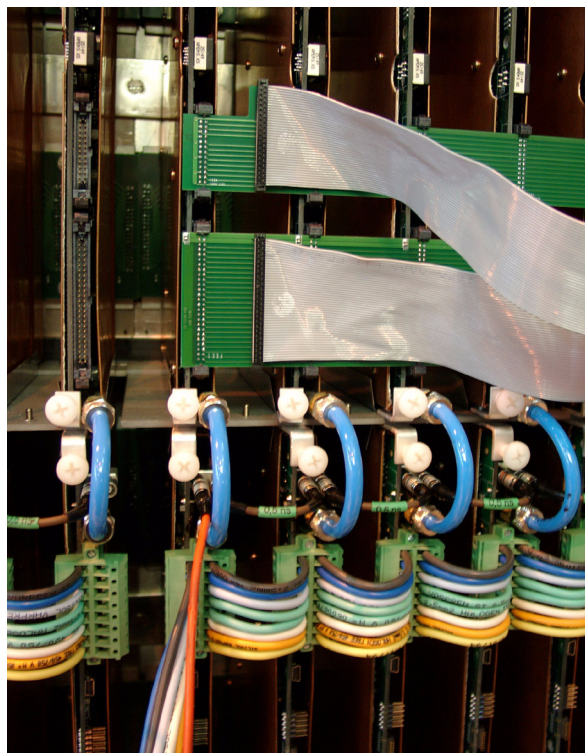


Figure 96 Detail of the LV power and RCU cable connection for FEE cards embedded in the PHOS module. The FEE cards are embedded within water cooled copper cassettes, the water pipes are high pressure plastic pipes (blue).

LV COLOR conventions

1. black +13.5V a
2. blue -6V a
3. grey +6V a
4. green A-GND
5. green D-GND
6. white +4V a
7. orange +3.3V d
8. yellow +4.2V d

The Low Voltage supply connections are differential between each Power-supply and the power patch panel (power block) on the PHOS module. Each differential power cable must be paralleled by sense wires since dynamic voltage changes due to high current can be considerable and are to be compensated at the power supply. The sense wires do this automatically and make sure that in case when FEE cards are disabled, or missing clocks, the Voltages at the FEE and RCU cannot become higher than allowed.

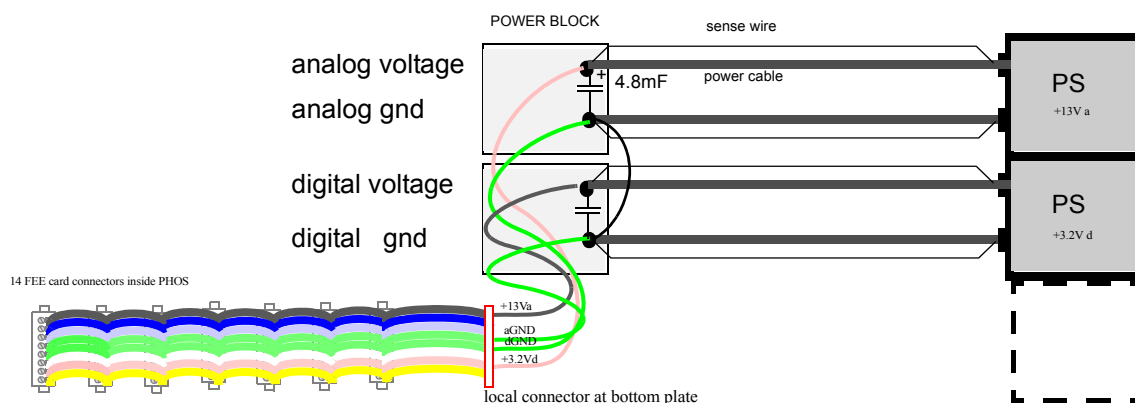


Figure 97 Connection schematics of 2 LV channels to external power supply

Figure 97 shows the connection schematics including sense wires and bulk filtering capacitors for analog and a digital voltages. The FEE card LV daisy chain is connected to the heavy LV cables via the intermediate power block(Figure 99).

The 4.8 mF capacitors in all supply lines protect the FEE electronics from dynamic overvoltages due to stopped readout clock or due to switching off all FEE cards at the same time.

The sense wires are only connected up to the power block since the drop over the local cables is considered low. Note that the analog and digital ground cables are 2 separate wires between the power block and the FEE chain. They are connected together for a common GND equipotential at each FEE card LV connector.

The logical LV connectivity and power plan for the FEE cards combined with the TRU and RCU's is

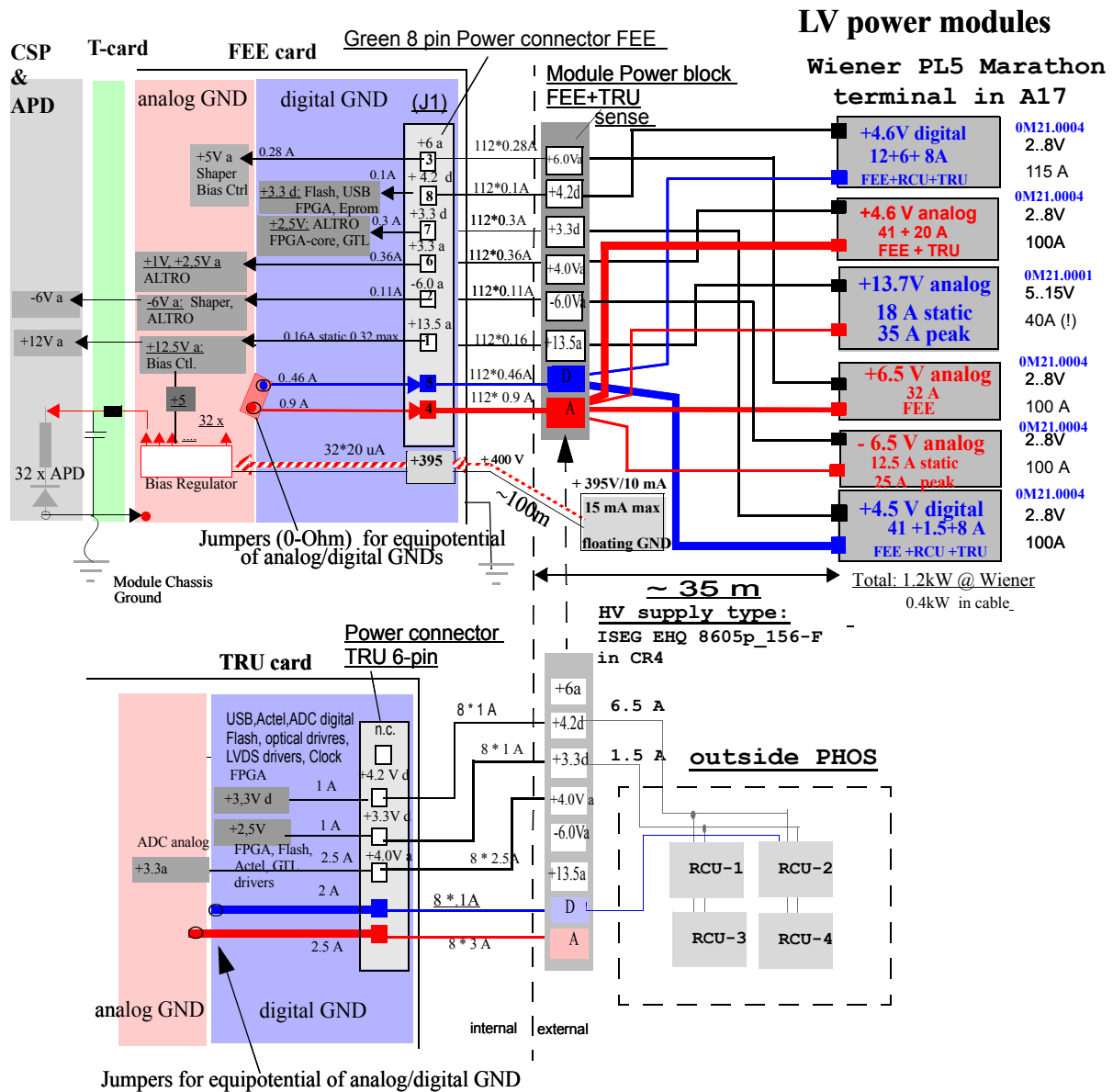


Figure 98 Power schematics for 1 PHOS module

detailed in Figure 98

The LV power supplies for 6 different Voltages are Wiener PL5 Marathon with individually regulable MEH modules per Voltage.

6 channels: 2 - 8 V - 115A / 600W type Wiener OM21.0004

12 channels: 5 - 15V - 22A / 300W type Wiener OM21.0001

For the floating power connection there are 2 * 6 power cables of 35 m length between the Power Supplies in A17 and the PHOS module. The power cable is a Fibernet cable of 150 mm² copper with 0.1133 milliOHM/meter, hence taking a worst case length of 40 m, the ohmic resistance per single cable is 4.53 milliOHM, and the differential voltage drop between the power supply voltage and PHOS is

$$\Delta U = 9.06 \text{ milliOHM} \times I$$

For example with 60 A, in order to maintain +4.0 Volt at the PHOS module, the Power Supply must provide 4.5 Volt. The power cables are attached at power blocks (see Figure 99) on the bottom plate of the PHOS from where the individual 14-way LV strands are connected via 6.3 mm FASTON connectors.

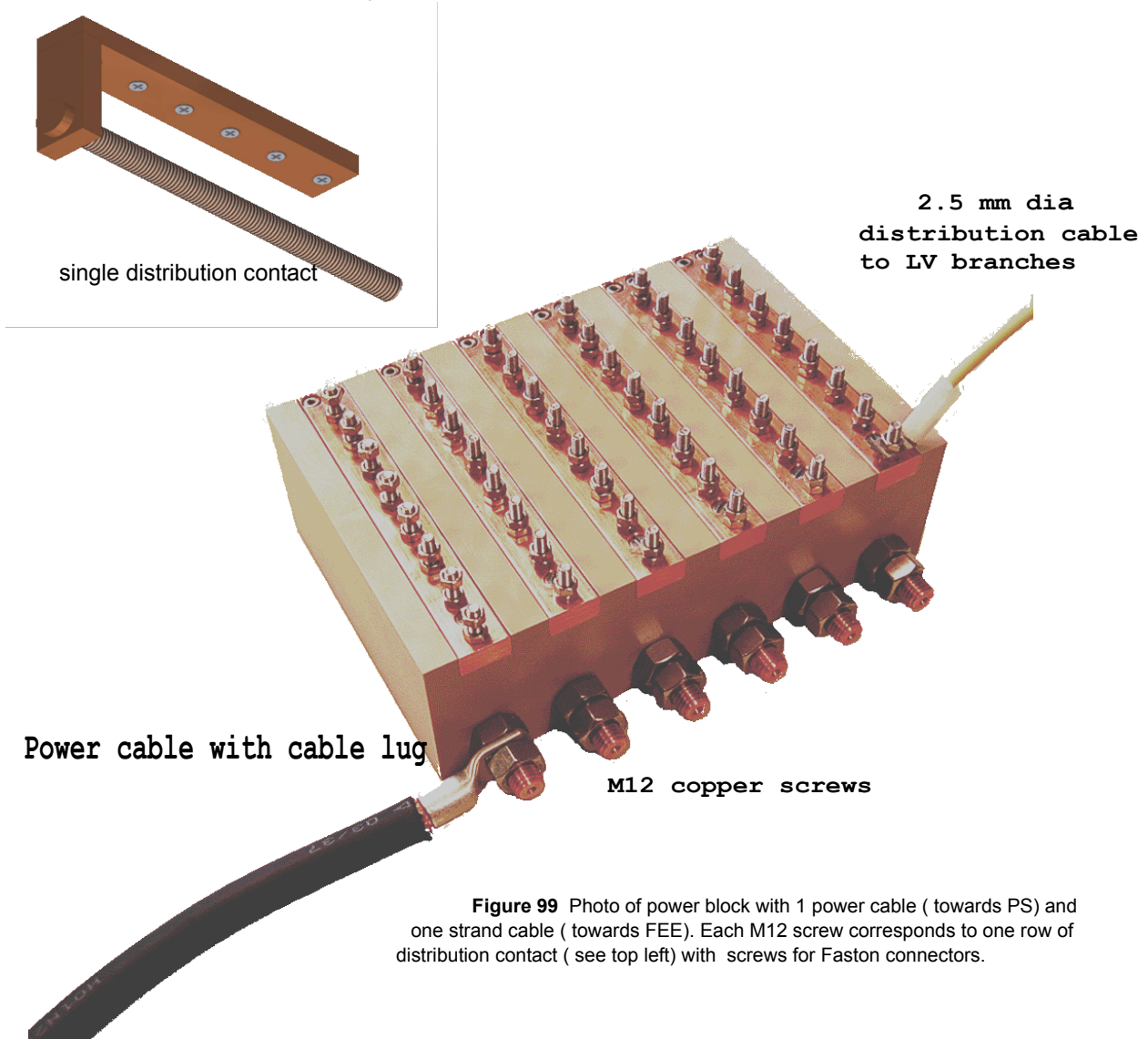


Figure 99 Photo of power block with 1 power cable (towards PS) and one strand cable (towards FEE). Each M12 screw corresponds to one row of distribution contact (see top left) with screws for Faston connectors.

13.1 Power connection to Wiener Power Supply

The Wiener Marathon supplies have a standard 2 x 12 row connection M5 screw panel and connectors for sense wires. In order to connect the thick 150 mm² cables via M12 bolts, a special backpanel was designed with intermediate wiring to the Wiener standard backpanel. Figure 100 shows some details how the Wiener

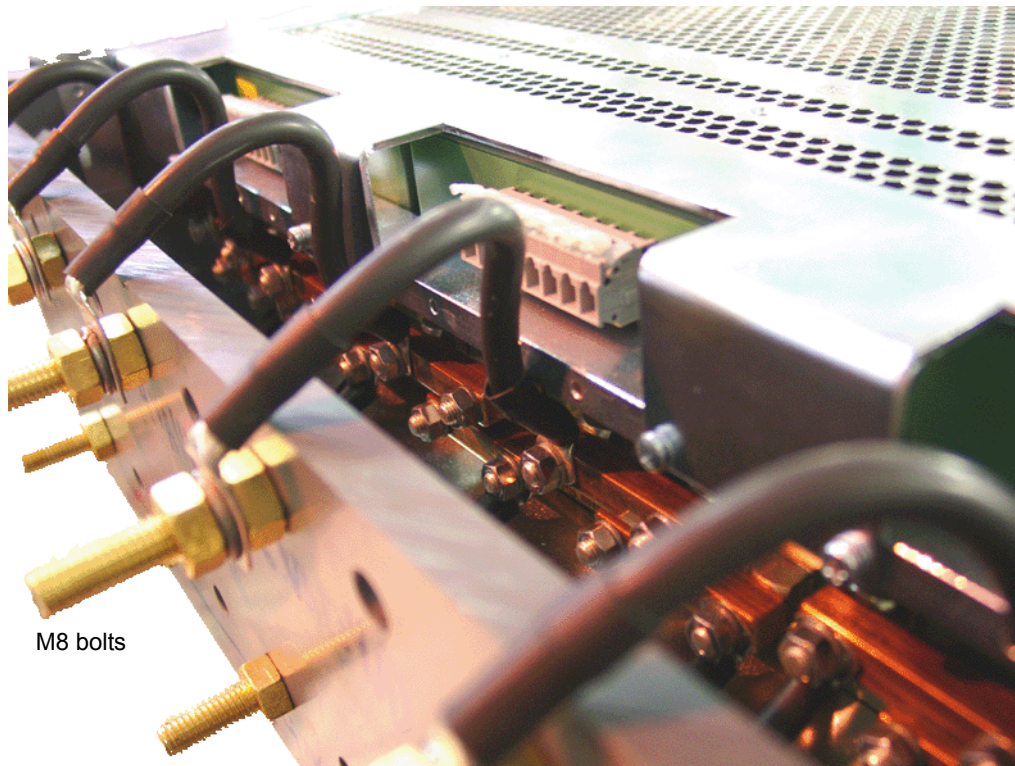


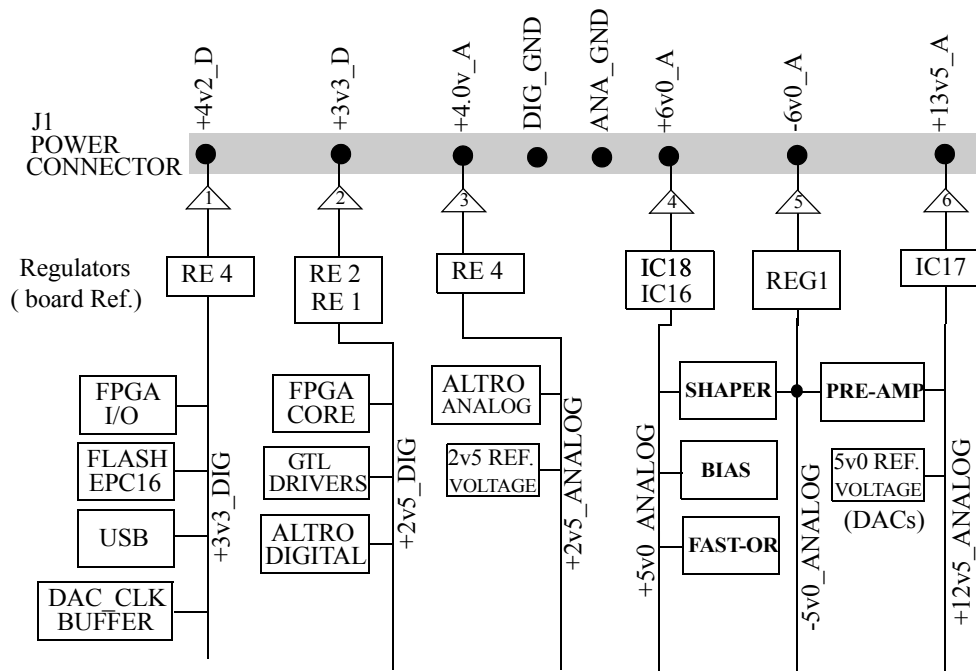
Figure 100 Wiener backpanel for 6 or 12 channel Supplies with rear power patchpanel.

backpanel is connected to the auxiliary power backpanel.

Note: 6 channel Wiener supplies require that pairs of M5 screw outputs are connected in parallel, (implemented via 7x7mm² copper bars).

13.2 LV supply hierarchy on FEE cards

The LV supply hierchies for the FEE card electronic sections is depicted in Figure 101. The designations



Voltage/ Current Sensors	Power Line	Values Stored on Registers of Board Controller			
		Voltage Registers		Current Registers	
		Mnemonic	Reg. Address	Mnemonic	Reg. Address
1	+4v2D	D4V2	07	D4V2C	08
2	+3v3D	D3V3	09	D3V3C	0A
3	+3v3A	A4V0	29	A4V0C	2A
4	+6v0A	A6V0	3B	A6VC	3C
5	-6v0A	AM6V0	39	AM6VC	3A
6	+13v5A	A13V5	2B	A13V5C	2C

Figure 101 LV Power hierarchies and Board Controller LV test registers on the FEE cards

of the regulators corresponds to the ones on the FEE cards. The Current/Voltage sense testpoints are depicted as triangles.

13.3 Low Voltage current/temperature/voltage monitoring

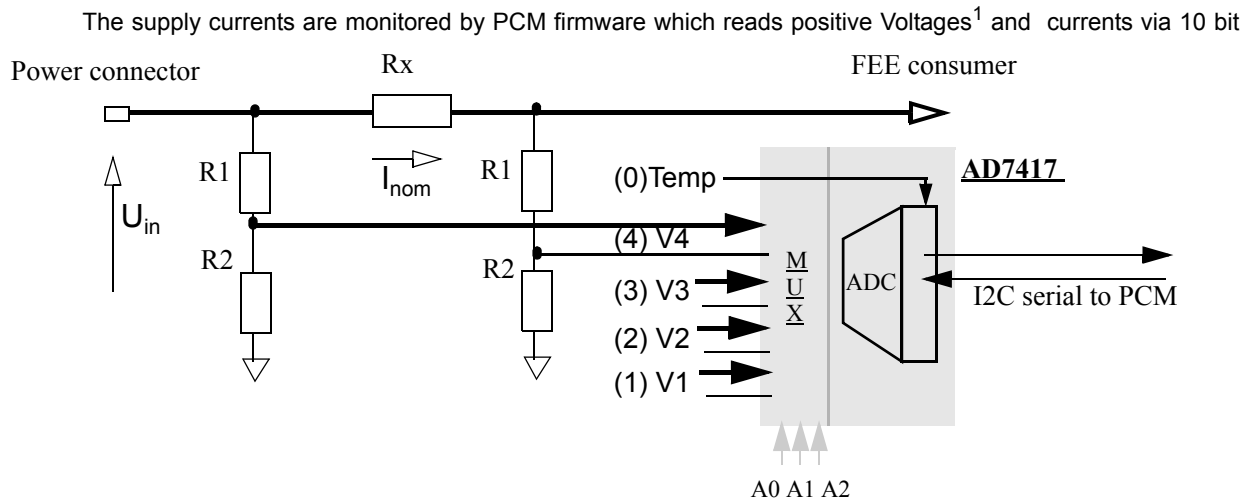


Figure 102 Onboard current measuring scheme with AD7417 10 bit ADC

ADCs of type AD7417, connected as shown in Figure 103. There are 3 such chips distributed over the FEE card (indicated in Figure 72): one on each side of the PCB between the Altro ADC's and one in the power regulator section. The three AD7417 chips (IC13, IC 14, IC15) measure also the FEE board temperatures.

The AD7417 data conversion can be initiated² by pulsing its *CONVST* input (corresponding to PCM address 0x1B). The standard PHOS monitoring mode of the AD7417 is however automatic periodic conversion. The two modes are selected via the bit 10 of CSR(0) at address 0x11.

1. the negative Voltage -6V is converted to effectively +2.2 Volt via an 8.2 Volt Zener diode.
2. 2 ms conversion time must be respected before reading the data registers

The data of the internal AD7414 registers (4 Voltages , 1 temperature per chip) are read out from the PCM via the I2C bus and mapped into PCM registers.

Table 5 T,V,I monitoring registers and conversion factors on the FEE card

Parameter	PCM register address	Conversion factor	Parameter	PCM register address	Conversion factor
Temp 1 (IC13)	0x06	0.25 C / count	voltage 13.5 V-A	0x2B	26.8 mV / count
voltage 4.2 V-D	0x07	8 mV / count	current 13.5 V-A	0x2C	22.3 mA / count
current 4.2 V-D	0x08	29.7 mA / count	Temp 3 (IC15)	0x38	0.25 C / count
voltage 3.3 V-D	0x09	6.4 mV / count	neg. voltage 6.0 V-A	0x39	4.88 mV/ count - 8.2 Volt
current 3.3 V-D	0x0A	43 mA / count	neg. current 6.0 V-A	0x3A	29.3 mA / count
Temp 2 (IC14)	0x288mV/bit)	0.25 C / count	voltage 6.0 V-A	0x3B	11.4 mV/ count
voltage 4.0 V-A	0x29	6.4 mV / count	current 6.0 V-A	0x3C	34.7 mA / count
current 4.0 V-A	0x2A	43 mA / count			

These AD7417 uses an internal 2.5 reference voltage, hence one bit corresponds to 2.441 mV. The AD7417 has four single-ended voltage inputs (channels 1-4) and one temperature monitoring channel (channel 0) which get selected by the Address lines A0,A1,A2 of the PCM..

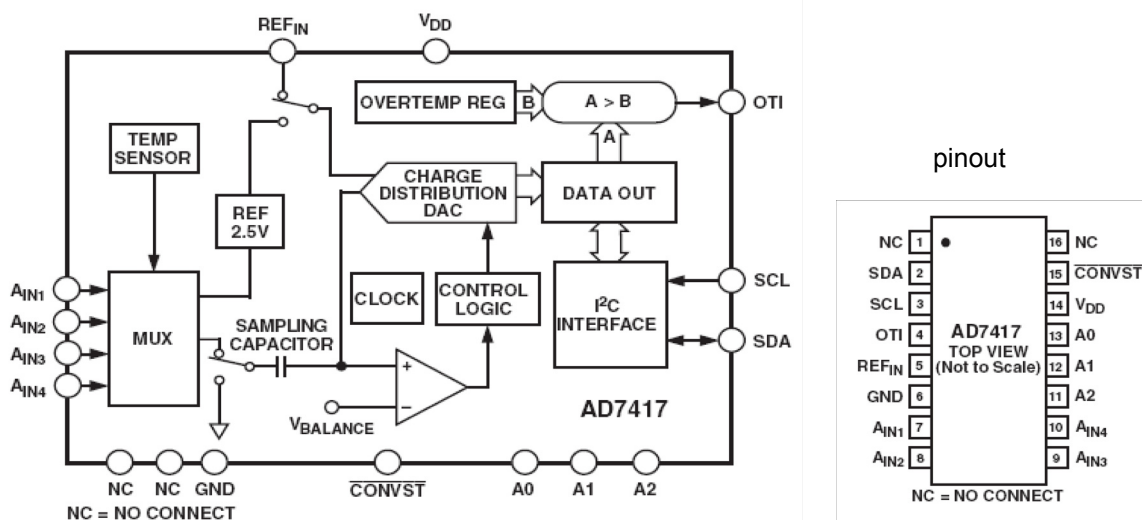


Figure 103 AD7417 functional diagram. It includes a 10 bit ADC with 4 multiplexed inputs and one temperature sensor with overtemperature flag output. Data are read out by the PCM via SCL/SDA of the I2C interface.

The PCM -based current measuring / surveillance scheme measures :

- a.) voltages from the FEE power connector multiplied by $R2/(R1+R2)$. There are two channels per AD7417 dedicated to Voltage measurements (see 13.3.1)

b.) the currents are measured as Voltage difference over the bypass resistors. Rx in each supply line. For each current, one pair of channels of the AD7417 is required since the current is calculated by the PCM as voltage difference $R_x \cdot I_{nom} \cdot R_2 / (R_2 + R_1)$.

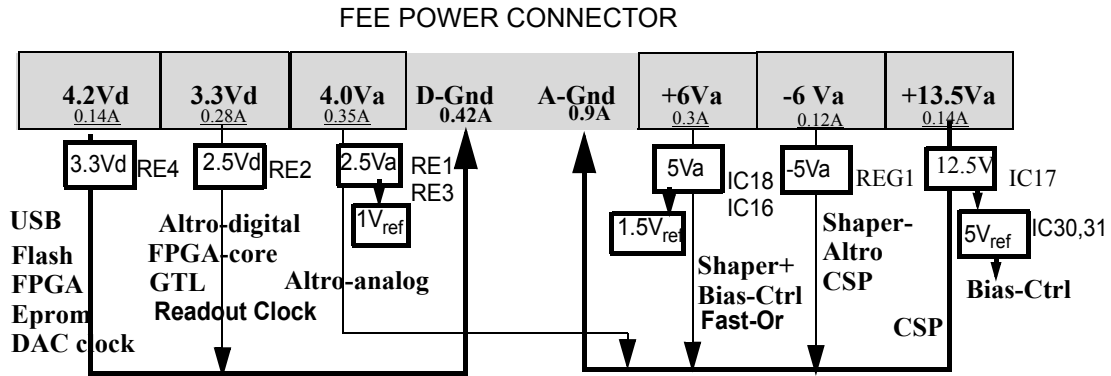


Figure 104 Supply voltages and currents of FEE card sections

The Rx resistors are arranged around the power connector as depicted in Figure 93. After resetting the FEE card into the default state, the nominal differential voltages measured over Rx are shown in Table 6,

Table 6 Current measuring as difference of 2 Voltage channels of AD7417

Input Voltage Voltage/ Rx on FEE card	I_{nom} {A}	R1	R2	Factor = $R_2 / (R_2 + R_1)$	Rx bypass Resistor value	Nominal Voltage over Rx	nominal Voltage difference Udiff	Nominal AD7417 current (Udiff/2.4 mV)
4.2V d / R91	0.14	R83=6. 19K	R84=2. 7K	0.3037	0R27	38 mV	11 mV	0x5
3.3V d / R 92	0.31	R85=4. 42K	R86=2. 7K	0.379	0R15	46.5 mV	17.6 mV	0x7
4.0V a / R 107	0.34A	R103= 4.42K	R104= 2.7K	0.379	0R15	51 mV	19.3 mV	0x8
+6 V a / R108	0.32A	R105= 10K	R106= 2.7K	0.213	0R33	105 mV	22.1 mV	0x9
-6V a / R87 ^a	0.12A	R97= 1K	R125=1 K	0.50	0R22	27 mV	13.5 mV	0x6
+13V a/ R94	0.14A	R89= 27K	R90= 2.7K	0.091	1R2	168 mV (FEE+CSP)	15.1 mV	0x6

a. Note that the negative voltage -6V gets converted into a positive voltage at the input of the ADC via 8Volt Zener diodes. Effectively, the -6Volt input is converted into a +2.2 Volt for the measurement.

The bypass currents monitored by the PCM should make sure that all currents stay below the nominal limits. The ADC voltages which correspond to the current limits should not overpass the nominal value by more than 20%. For readings beyond limit, the PCM generates an interrupt to the RCU which is recognized by the monitoring and safety module of the RCU (if enabled). Depending on the severity of the interrupt, the RCU can switch off the FEE card which generated the interrupt.

For reading of the T,V,I values when the data bus is busy with data transfers, the serial protocol between RCU and PCM is available.

13.3.1 PCM Voltage / current measurement

The ADC counts of the Voltage measurements on a single FEE card correspond to 2.441 mV per bit, however have to be corrected with the voltage divider factor $R2/(R2+R1)$, hence:

- +4V2d --> 1.27 V, measured value 0x208 -> 0.14 A, measured value 0x5
- +3V3d --> 1.25 V measured 0x200-> 0.31 A, measured value 0x7
- +4V0a --> 1.52 V measured 0x26E-> 0.34 A, measured value 0x8
- +6Va --> 1.27 V measured 0x208->0.32 A, measured value 0x9
- -6Va --> 1V measured 0x199->0.32A, measured value 0xE
- +13Va --> 1.18 V measured value 0x1E3->0.14A, measured value 0x6

13.3.2 PCM Temperature Measurement

For conversion of the channel 0 temperature reading into Celsius the reading has to be divided by 4. (this is valid for positive temperatures)

The temperature equivalences of 10 bit readings are shown below for 4 temperatures: The temperature is a linear function of readings, obtained as ADC counts divided by 4.

- +10 C = 00 0010 1000 (0x28)
- +25 C = 00 0110 0100 (0x64)
- +50 C = 00 1100 1000 (0xC8) values above 0xC MUST set an interrupt
- +75 C = 01 0010 1100 (0x12C)

On-chip registers of the AD7417 can be programmed with high and low temperature limits, and an open-drain overtemperature indicator (OTI) output is provided, which becomes active when a programmed limit is exceeded.

Overtemperature above 40 C must generate an interrupt to the RCU.

13.3.3 Conversion of AD7417 readings

With the previous chapters, the conversion equations for the ADC readings AD7417 are:

- Temperature [C] = ADC-reading /4
- positive Voltage [V] = ADC-reading *2.441 mV / Factor
- negative Voltage [V] = ADC-reading *2.441 mV / Factor - 8.2 Volt
- Current [I] = ADC-reading *2.441 mV / Rx / Factor

13.3.4 PCM register access to AD7417

The current and temperature readback values and thresholds are accessed in PCM registers defined in the PCM manual [9]. The Nomenclature is

D4V2C = means Digital, 4.2Voltage, Current register

AM6V0 = means Analog, Minus 6.0 Voltage, Voltage Register

Some registers are listed in Table 724. For the complete PCM register and functional description see [9]

Table 7 some PCM registers for one thre AD7417, for complete PCM register map see [9]

PCM Address (hex)	Memnonic	Register Name	No. bits	access	Meaning
01	T1_Th	Temperature threshold T1	10	R/W	temperature theshold T1
06	TEMP1	Temperature 1	10	R	Temperature value IC13
07	D4V2	4.2 Volt digital voltage	10	R	4.2 Volt digital reading IC13
08	D4V2C	current of digital 4V	10	R	Current of 4 Volt line IC13
09	D3V3	3.3 Volt digital voltage	10	R	3.3 Volt digital reading IC13
0A	D3V3C	current of digital 3.3 Volt	10	R	current of 3.3Volt IC13
21	T2_TH	Temperature threshold T2	10	R/W	temperature theshold T2
22	AM6V_TH	AM6V Threshold	10	R/W	Min. -6V analog threshold
23	AM6VC_TH	AM6VC Threshold	10	R/W	Max -6V analog current threshold
24	A13V_TH	A13 Volt threshold	10	R/W	Min. Voltage +13 V analog
25	A13VC_TH	A13 Volt current thershold	10	R/W	Max. current of +13V analog
28	TEMP2	Temperature 2	10	R	Temperature value IC14
29	A4V0	Anal. Voltage 4.0V	10	R	4.0 V analog Voltage value IC14
2A	A4V0C	Current anal. 4.0V	10	R	Current of 4.0 Volt analog IC14
2B	A13V5	+13 Volt analog Voltage	10	R	13 Volt analog Voltage IC14
2C	A13V5C	13V current	10	R	Current on +13 V analog line IC14
31	T3_TH	Temperature T3 threshold	10	R/W	Max temperature threshold T3
32	A3V3_TH	A3V3_Thershold	10	R/W	Min 3.3V analog threshold
33	A3V3C_TH	A3V3 Current threshold	10	R/W	Max. 3.3 V analog current theshold
34	A6V_TH	A6V Voltage Threshold	10	R/W	Min analog 6V threshold
35	A6VC_TH	A6VC Current threshold	10	R/W	Max analog Current 6V
38	TEMP 3	Temperature 3	10	R	Temperature IC15
39	AM6V0	-6V analog Voltage	10	R	-6Volt analog Voltage IC15

Table 7 some PCM registers for one thre AD7417, for complete PCM register map see [9]

3A	AM6V0C	current of -6V analog	10	R	Current of -6V analog IC15
3B	A6V0	6V analog Voltage	10	R	6 Volt analog reading IC15
3C	A6V0C	current of 6V analog	10	R	current of 6V analog IC15

Note: *the AD7417 Voltage and Current readings in the first FEE card production are not very precise (20 %) due to tolerances of the resistors Rx and R1,2,3, 4, used for the measurement on the FEE cards. For new FEE production, bypass resistors Rx and voltage divider resistors R1-R4 should have a tolerance of 1 %.*

The temperatures are relatively precise since they are read directly from the AD7417.

The example in Appendix 2. shows testing of the AD7417 registers via DCS script for branch A and FEE address Nr 4.

14 Power Enabling / Controls logic on FEE [6]

The Power on the FEE card gets enabled or disabled via the “card-switch” signal on the GTL bus (see Figure 108 and Figure 208) which is issued by the RCU¹ according to the Front End Card Active List (FEC AL) definition. Similarly FEE cards are read out by the RCU according to the readout list (RDOL). The monitoring and safety module can however remove FEE cards from the FEC and RDO list if interrupts are enabled and received (see 15.5). Therefore, in cases where FEE card power cannot be enabled on individual cards it may be possible that FEC list was modified by the RCU due to a problem which was generated via an interrupt.

Note: the most frequent case of un-successful FEE enabling is that the card is situated on the wrong RCU branch or the fact that the enable bits are shifted by 1 with respect to the TPC situation. **The RCU firmware must be enabled to <PHOS mode> by setting register 0x8009 to “1”.**

14.1 Front End Card enabling

In order to enable power on FEE cards via the RCU, a command line in the reset script defines the “FEC AL” via the control register at address 0x8000. The lower 16 bit correspond to branch A, whereas the higher 16bit correspond to branch B.

Note: Branch A the the branch connected on the RCU on the same side as the (metallic) FPGA see Figure 91

A bit is set to “1” to enable the corresponding FEE card (see Figure 105). The corresponding (ReadOut List =RDO) is to be stored on the RCU register at address 0x8001. Note that for PHOS, the address coding places the TRU at address 0x1 and the first FEE card at address 0x2.

Example:

w 0x8000 0x0000000F # FEC AL enables TRU (#0) and FEE cards #1-3 on Branch A

w 0x8001 0x00000002 # RDO defines readout of FEE card #1 on Branch A

The “card switch” signal enables FEE cards via R110 in Figure 108. The individual card switch signals are routed via the GTL control bus to each geographical position of an FEE card.

Note: Since there are only 13 enable signals foreseen by the original TPC RCU design (compare Figure 107), for PHOS FEE cards the geographical addresses 1 + 13 and 2 + 14 are connected together !

For this reason, the FEC AL initialization has to take into account the special grouping for the PHOS detector. Some Examples:

w 0x8000 0x00000002 # Set active Front End Card list for FEE cards #1 and #14, Branch A

w 0x8000 0x00020000 # set active Front End Card list for FEE cards #1 and #14 on Branch B

1. or in TEST mode by USB

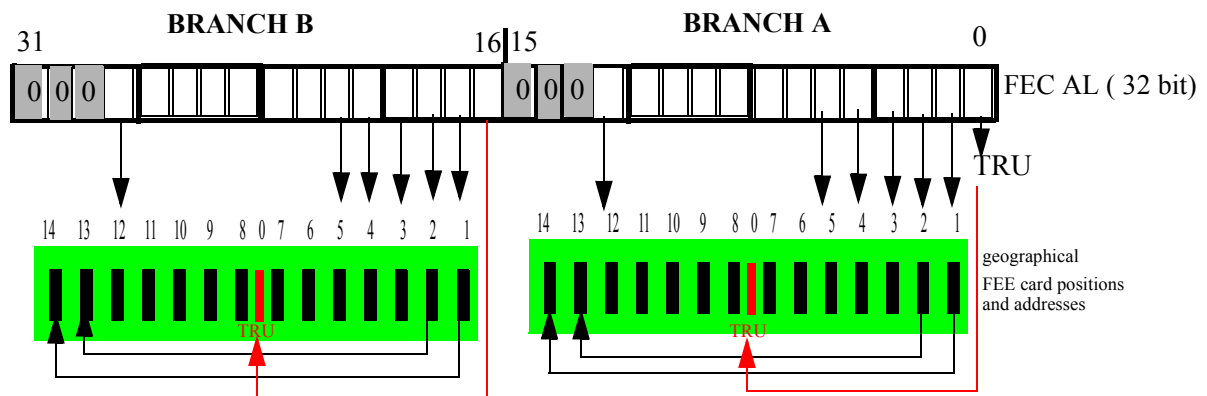


Figure 105 PHOS FEE card geographical correspondence with software list enabling

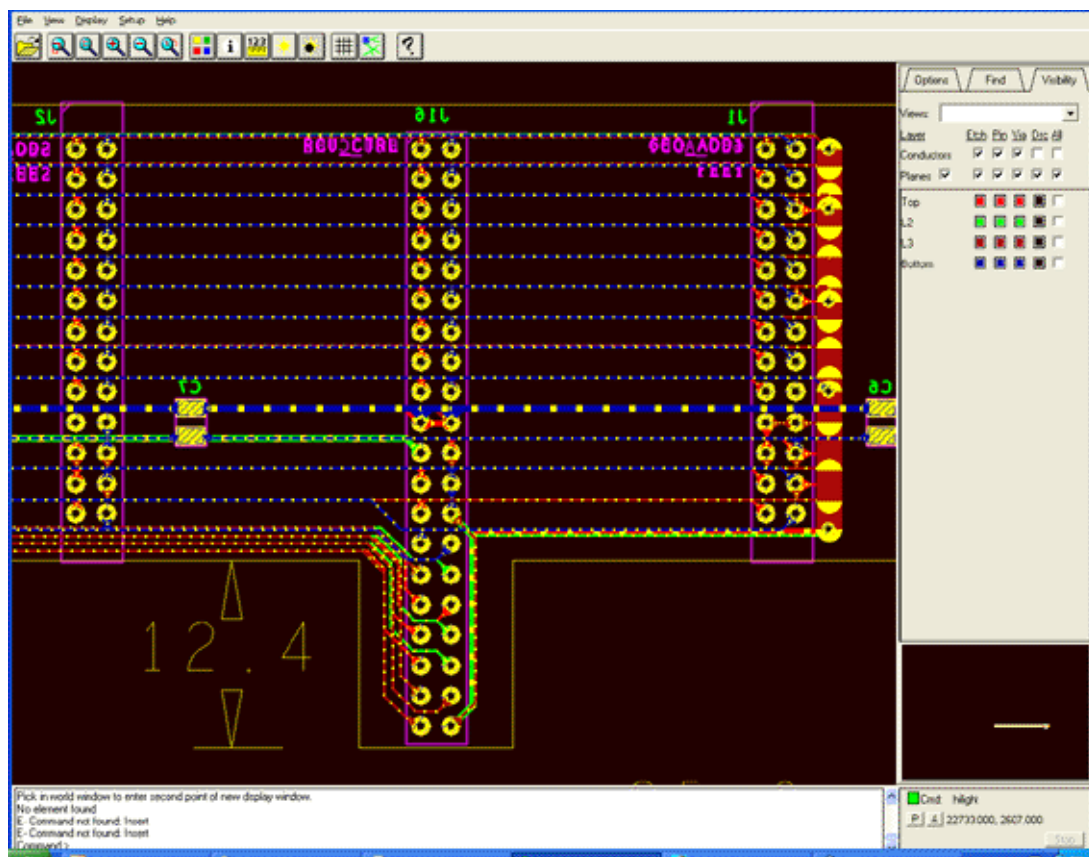


Figure 106 40 pin cable connector to the 26 pin GTL control bus. The FEE connectors are 30 pin connectors of which 4 pins are removed (2 on each side) The extruding 40 pin cable connector section contains the 12 individual card enable signals of the RCU which are routed to the individual card connectors. **Note:** Two card enable signal pairs (1,14 and 2,13) are connected together on the current GTL bus strips. Card enable 14 and 13 should be connected to pin 27 respectively in future GTL bus versions to allow enabling/disabling of FEE cards 14 together 13 independently of card 1 and 2.

The control buses A and B mastered by the RCU consist of 40 lines, of which only a subset of 26 are routed

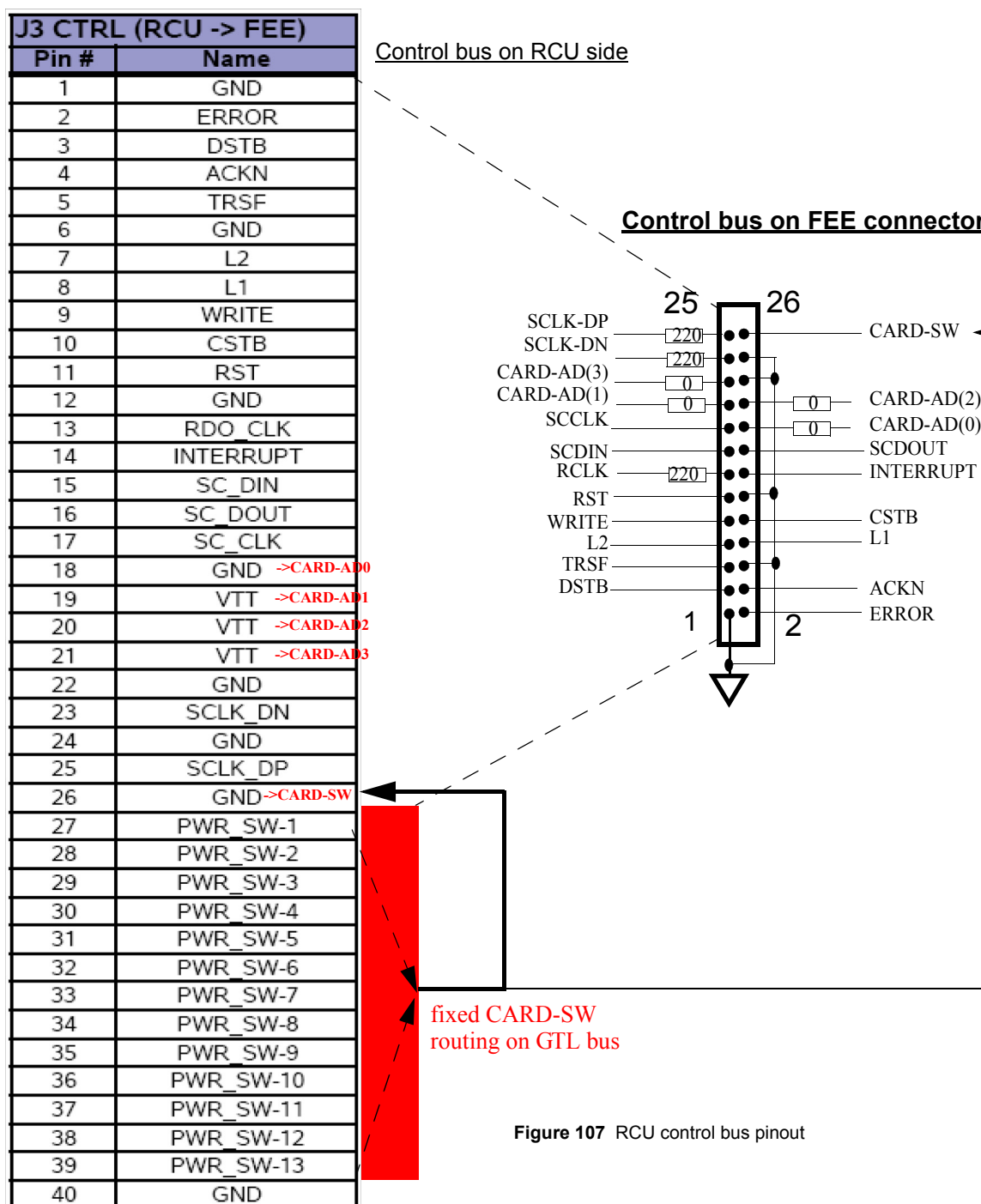
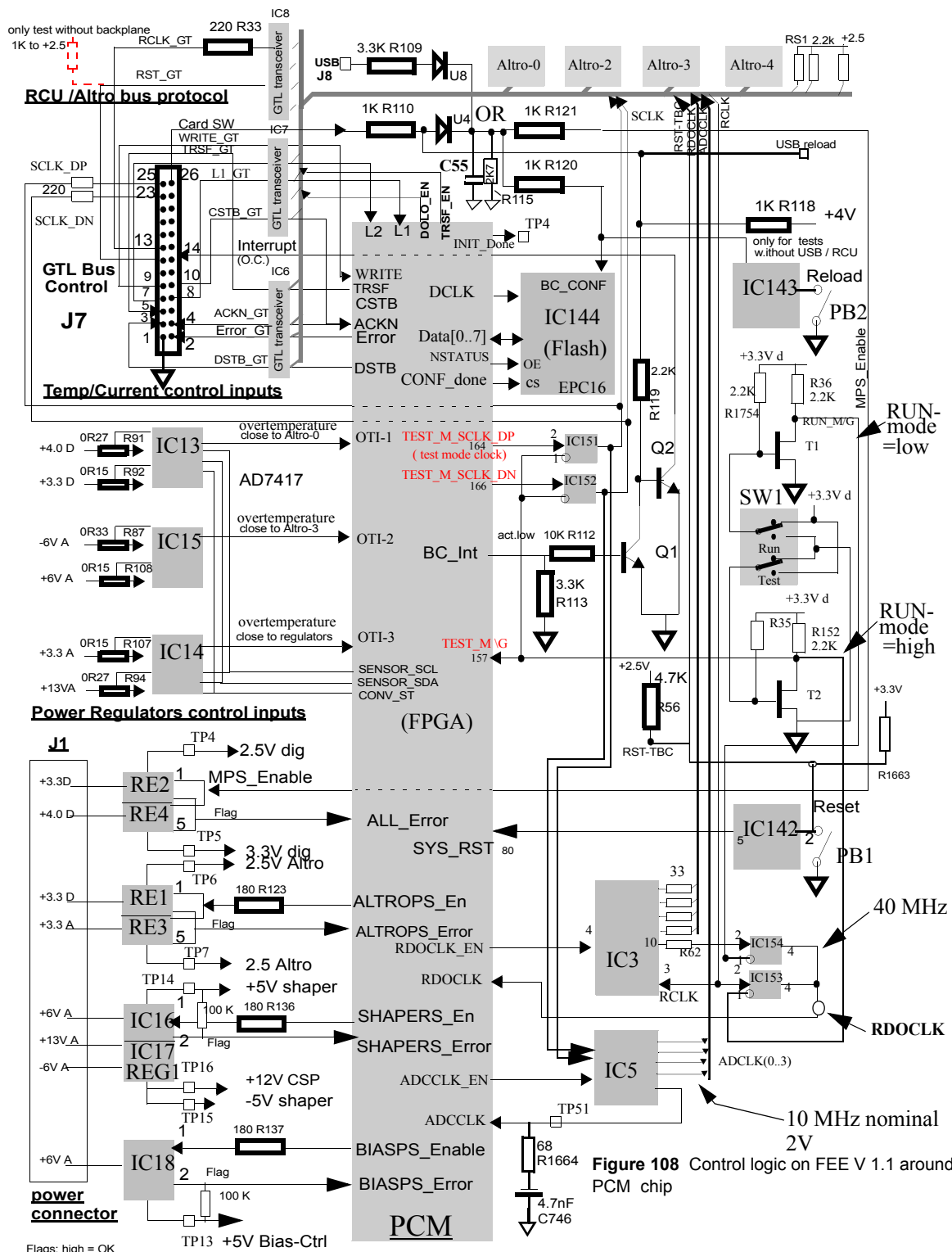


Figure 107 RCU control bus pinout

to each FEE or TRU card. (Figure 107 and Figure 107). More precise details of the power enabling logic are shown in Figure 108. For full information, the FEE card schematics need to be consulted (to be found in EDMS under Alice Engineering Baseline / PHOS Spectrometer/Alice PHOS FEE) As an overview, Figure 108 is a “simplified schematics” of the control logic around the PCM controller.

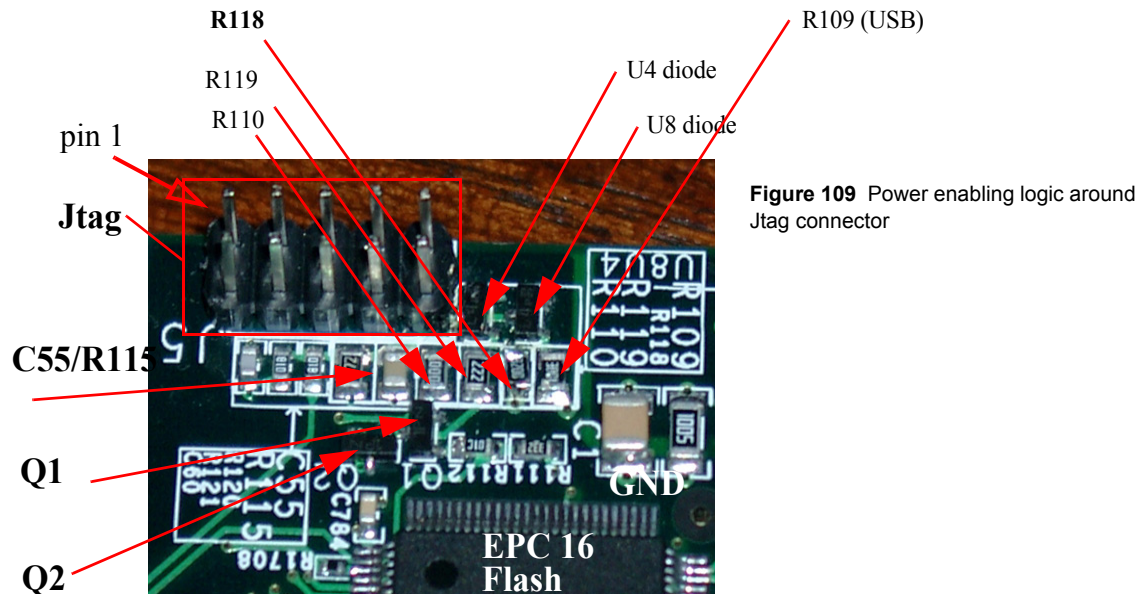
The FEE digital power is enabled by an analog OR from 2 sources: RCU master or USB master.



On availability of the card-enable signal, the enabling logic generates the signal MPS_Enable, which enables the digital voltages 3.3 V and 2.5 Volt (TP4 and TP5) required by the digital part (including PCM) of the FEE

card. The other supply voltages (Altro, shaper, bias control) are enabled by state machines of the PCM logic which can disable these parts in case of over-temperature or over-currents, measured by IC13,14, and 15.

The position of the crucial components for the FEE power scheme are shown in Figure 109.



14.2 System Reset

A 6 ms system reset pulse is generated on power-on, or via the reset pushbutton, or via the reset command

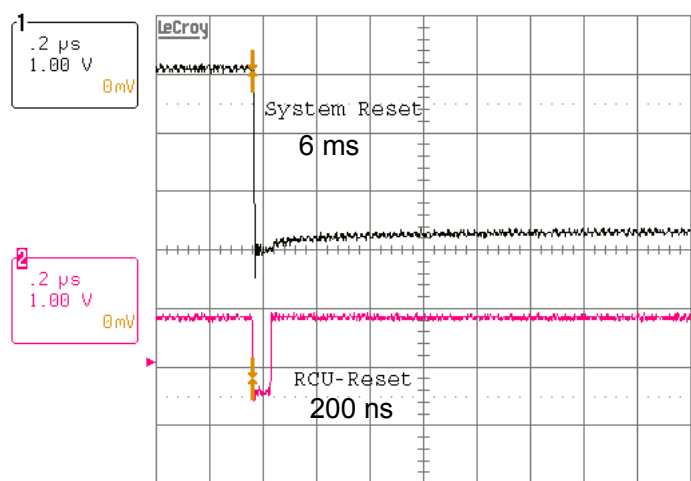


Figure 110 RCU reset pulse generates a long-duration System reset pulse.

on to FEE cards. The active circuit which produces the reset pulse is IC 142 of type TLC7733. The timing elements for the reset pulse length are the capacitors C 741,742,743, connected in parallel with a value of 100 nF each.

The software RESET is executed as as script on the DCS card and initializes the RCU and the FEE cards:

The reset sequence (see 15.3) includes wait commands in order to allow for the relatively long reset pulse duration. The reset pulses as shown in Figure 110 are generated by accessing the address 0x2001

15 PCM Control and Monitoring firmware [9]

The PCM controller¹ on the FEE cards are firmware state machines which respond as slave device to the DCS subsystem of the Readout Control Unit (RCU). The default communication protocol is via the parallel GTL bus. For an independent control communication whilst the GTL bus is busy (during runs), the PCM implements also an I2C-like serial RCU protocol (implemented via the GTL bus). Either of both protocols connects all FEE cards with the control domain of the RCU (see Figure 111).

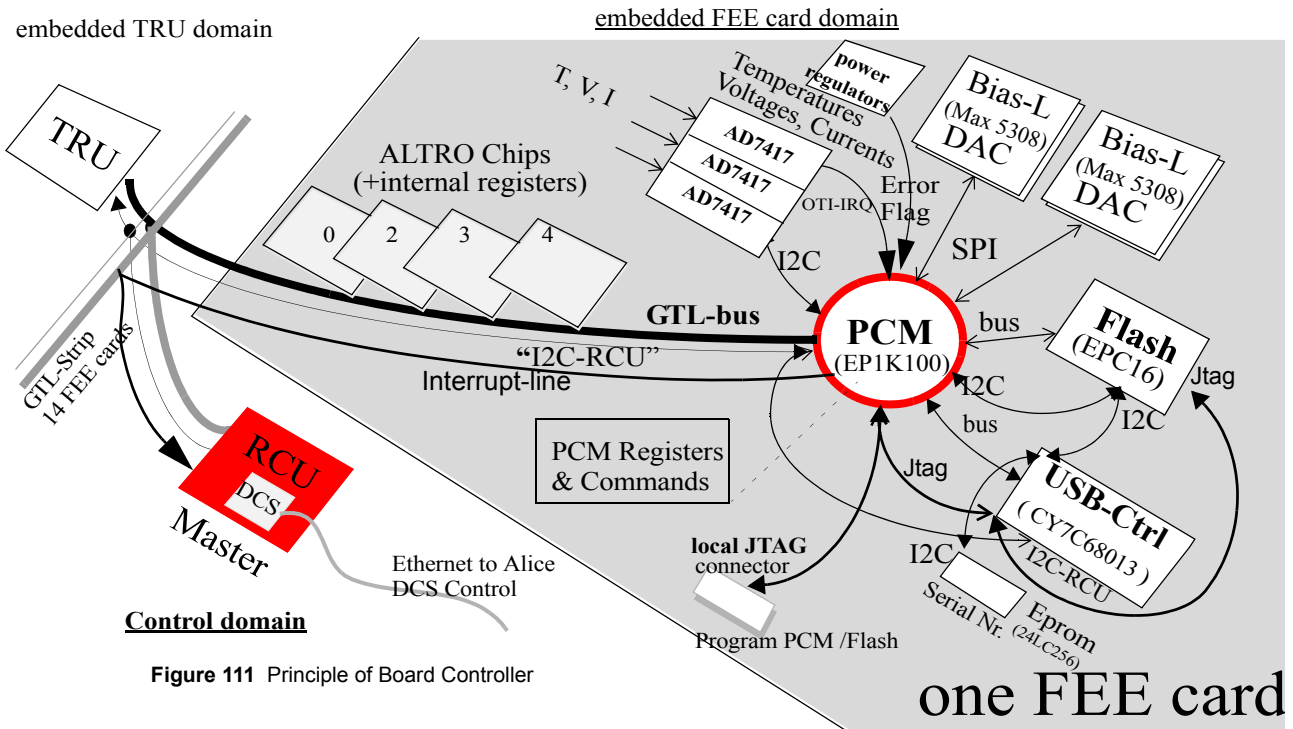


Figure 111 Principle of Board Controller

The PCM either mirrors the status of values in a set of monitoring registers or it uses a register to update setting for peripheral logic around the PCM. It also drives line protocols like Reset (see chapter 30), Interrupt (see chapter 15.5) or error (see chapter 15.6). The Altro chips receive and send their data directly via the parallel GTL bus. The communication between the RCU and the PCM registers is through either the RCU-I²C protocol or through the GTL bus. The PCM by itself communicates with the monitoring ADC's (AD7417) via I2C and with the Bias Control DACs via the Motorola SPI bus. On power-up, the PCM FPGA is loaded from the Flash which can be programmed via the JTAG bus via external programmers like the Altera Byteblaster. The FPGA can be directly re-programmed via JTAG bus, however it will be re-configured on power-up from the Flash.

The board control logic on the PHOS FEE card was originally based on the Board Controller on the TPC FEC card. The PHOS PCM includes 32 additional registers for the APD bias setting and the Motorola SPI bus for the APD bias regulation. It receives also prompt error flag lines from the power regulators and from the temperature warning flags of the AD7417s.

For local board diagnostics (without RCU), both the FEE and the TRU are equipped with a single-chip USB port, which maps on one side into the I2C bus between PCM, Flash and serial Eprom, on the other side to the I2C-RCU protocol. In this way, all register resources which are available on the RCU via I2C could be used also via a USB connection to a local PC. In particular the Eprom which contains the serial Number can be programmed via USB.

1. previously called Board Controller, renamed PCM to avoid confusion with the TPC Board controller

The USB controller on the FEE card is planned to be used for local servicing via a standard PC. It includes a micro-processor with programmable parallel ports and a native Jtag port. The parallel ports are meant to be used for FiFo based data exchange with the PCM and for serving the I2C protocol.

Figure 112 shows details of the PCM internal structure and interface logic.

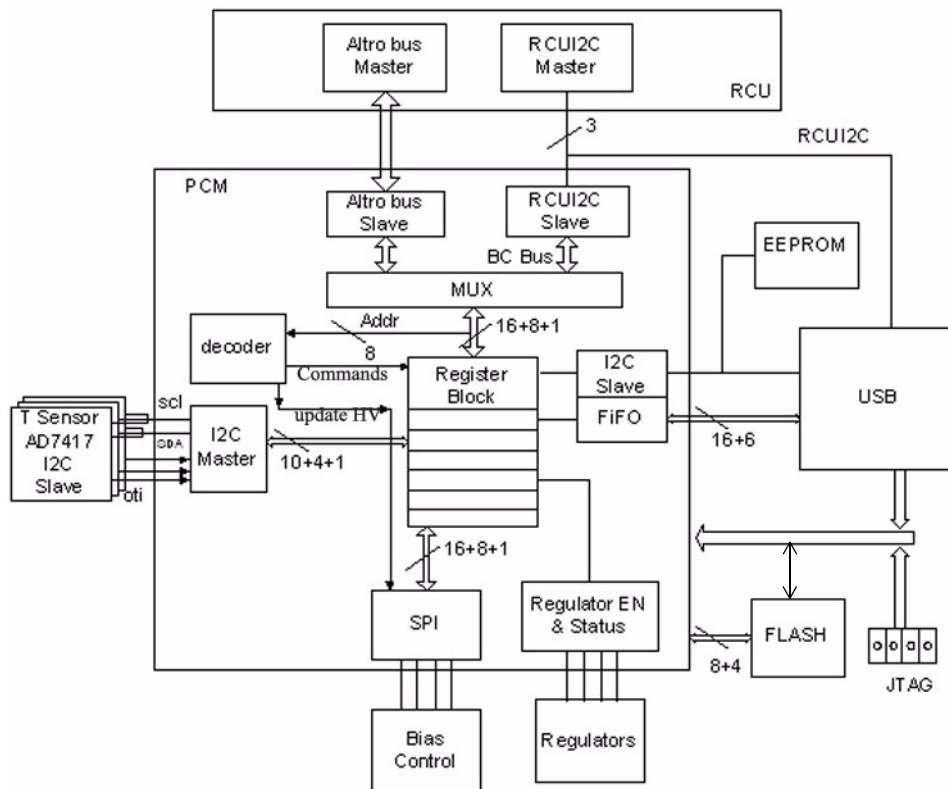


Figure 112 Details of Phos Control and Monitoring logic (PCM)

The PCM communication with RCU goes either via the Altro slave port of the PCM or via the RCU-I2C slave port of the PCM. The PCM register block contains control registers and registers which allow to write/read the registers of its peripherals (AD7417 and bias DACs) directly via their I2C master and a SPI ports. The PCM receives status flags from the power regulators and from the AD7417 over-temperature flag (OTI). A set of registers control the APD BIAS control logic via the serial SPI bus to the DACs of the BIAS Control logic. The USB port for data transfer to the PCM is implemented as command Fifo.

15.1 Run and Test mode schemes

The switch SW1 selects one of 2 modes: Run mode and Test mode. The main mode is the Run mode and must be always selected whenever the RCU and other FEE cards are plugged into the backplane. Test mode is used when there is no backplane present. The Run/Test selection logic is shown in Figure 113

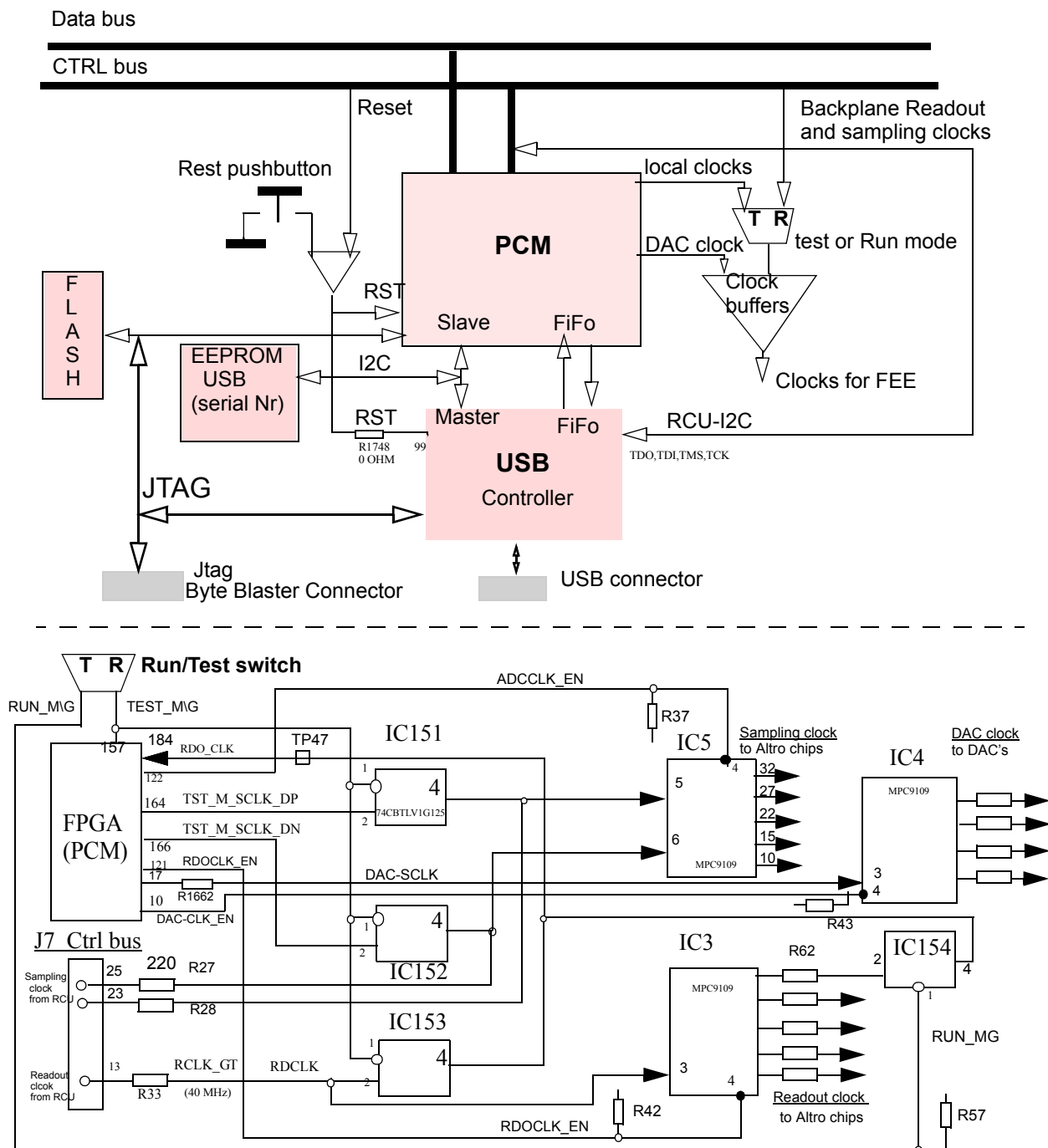


Figure 113 RUN and TEST mode selection on the FEE cards

15.2 Masterhip hierarchy

Figure 114 shows the PCM logic in a more global context within the DCS ->RCU ->FEE hierarchy. The DCS

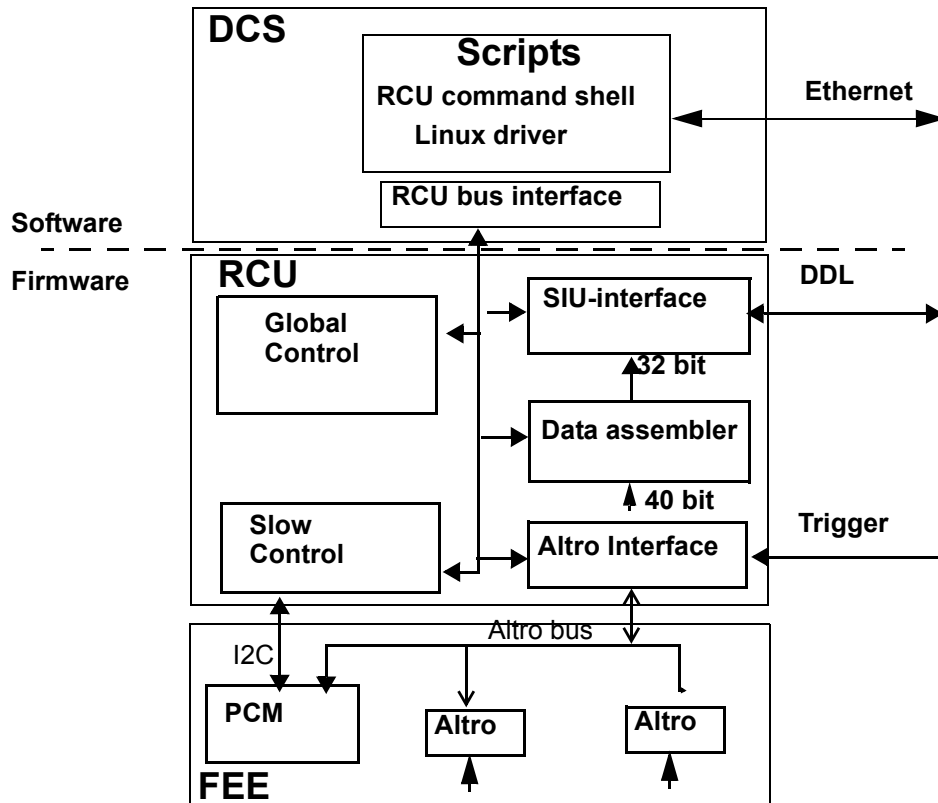


Figure 114 Location of PCM in Front-End Electronics of PHOS

linux processor is the master of the hardware RCU. The RCU is bus master of both the serial PCM control bus and of the parallel Altro bus.

The top level DCS command list for reading the version of the PCM is shown below (the PCM version number resides in the PCM register of address 0x20.) The example below shows how to read the PCM version number.

```

w 0x7000 0x523020      # read instruction to read the PCM version from FEE address 3 on branch A
                        # PCM address 0x020

w 0x7001 0x524020      # store another read instruction to read the PCM version from FEE address 4
w 0x7002 0x390000      # terminate the instruction list in the instruction memory

wait 1 us

w 0x0 0x0              # execute the script starting from instruction 00
                        # on the GTL bus, one must see and CSTB -> ACKN sequence

wait 1 us

r 0x7800               # check error and status register ( must be 0 )
r 0x6000 2             # list the two results of read instruction from 0x6000
0x12
```

```

0x12          # display of the PCM version number ( 0x12 for the current version 1.2)
w 0x6C01 0x00 # clear the error status register just in case ..

```

15.3 RCU initialization for PHOS

In order to program the RCU Xilinx FPGA from the Actel FLash memory, the following command needs to be executed on the DCS card:

```
w 0xb000 0x4
```

The common RCU firmware for PHOS and TPC requires that the *PHOS mode* with different addressing scheme is initialized via the command:

```
w 0x8009 0x1
```

Note: After RCU power-up, this command set is the first instruction to be executed before applying power to the FEE cards

The standard Reset script for PHOS is as follows:

```

w 0x2002 0x0 # reset both RCU and FEE
wait 1s
wait 1s
w 0x2002 0x0 # reset both RCU and FEE
wait 1s
w 0xe000 0x0 # make DCS card master
wait 1s
w 0x8009 0x1 # PHOS backplane version
wait 1s

```

15.4 Monitoring and safety module[24]

The Monitoring and safety module is firmware in both RCU and PCM which monitors critical parameters such as temperature (T), voltages (V) and currents (I), in order to generate maskable interrupts which are handled by the RCU according to severity and which are reported to the DCS.

As soon as one of the FEE parameters:

-Temperature as measured by the AD7417

-Current and voltages as measured by the AD7417

-Error Flag by the Voltage regulators

goes above range as defined in PCM registers, the PCM can assert the interrupt via the BC_INT line (see Figure 122). The condition is that interrupts are enabled in the Intmode register and that the individual error sources are not masked in the CSR(0) register of the PCM.

On interrupt detection, the RCU starts polling CSR(1) register of each FEE (according to the FEC list) in order to identify the error source. In order to serve the interrupt in real time, the RCU uses the serial RCIU-I2C protocol. The resources of interrupts on the FEE card are depicted in Figure 115 below.

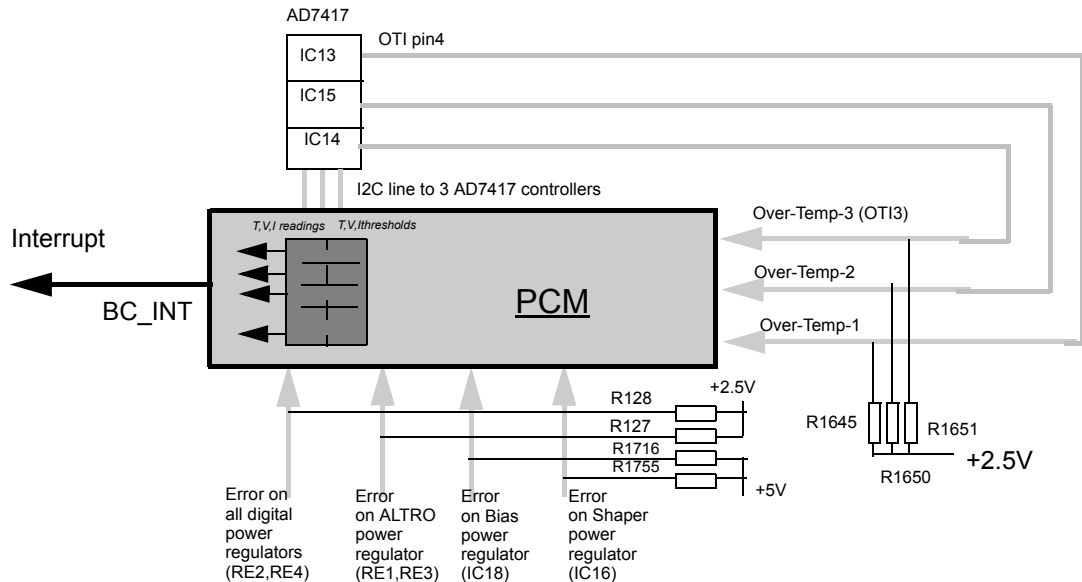


Figure 115 Sources of Interrupt for PCM

There are 3 overtemperature flag signals (OTI) from the 3 AD7414 chips, 4 error flags from the Voltage regulators (compare Figure 108) and the internal readings of the AD7414 Voltage, Current and Temperature readings which are always compared to their corresponding threshold registers as defined in Table 7.

In the event of an interrupt due to a hard error (overcurrent, overvoltage) the RCU switches off immediately the corresponding FEE. In case of a soft error (undervoltage, voltage regulator error flags) . The interrupt history is reported to the DCS system, allowing users to diagnose and cure the problem. In case of a soft interrupt, the corresponding FEE card is not switched off but removed from the readout list.

15.5 Interrupts [24]

The RCU interrupts are implemented as part of the PCM security module to detect spontaneous problems in the FEE cards, such as rapidly developing temperature (T), voltage (V) or current (I) problems. Slow variations can also be monitored without interrupts by reading the corresponding T,V,I registers of the AD7417 sensors (Table 5) via the parallel or serial interface

Note: RCU interrupts can automatically remove FEE cards from the active card list and from the readout list.

The interrupts are enabled via the RCU 2-bit INTmode register at 0x8004. Bit 0 enables interrupts for Branch A and bit 1 enables the interrupts for branch B.

Example:


```
enter operation (h/i/q/r/w):w 0x8004 0x1      #Enable interrupt of Branch A
```

(Now an Interrupt is generated by heating up theAD7417 chip above 40 C)

```
enter operation (h/i/q/r/w): r 0x8100 32      #Read values of the RCU interrupt status memory
0x8100: 0x2 0x1001 0x8000 0      # 2 interrupts, 0x1001 means branch A, address 4, temp > t_th
0x8104: 0 0 0 0
0x8108: 0 0 0 0
0x810c: 0 0 0 0
```

In this example the fact is used that all interrupts are enabled by default in the 8 bit interrupt mask of CSR(0). The interrupt status memory starts with entry 2 for the two subsequent recorded interrupts. The first 0x1001 reports a hard interrupt, the second 0x8000 an un-identified interrupt. For disabling specific interrupt sources, the corresponding mask bit is to be cleared.

Interrupts work with the status registers CSR(0) for interrupts masks at PCM address 0x11 and with CSR(1) for Error and Interrupt Flags at PCM address 0x12. The RCU status memory at 0x8100 records up to 32 interrupts with detailed information about the interrupt source.

Interrupts on the PHOS FEE are generated on reasons which are summarized as interrupt flag bits, shown in Figure 116:

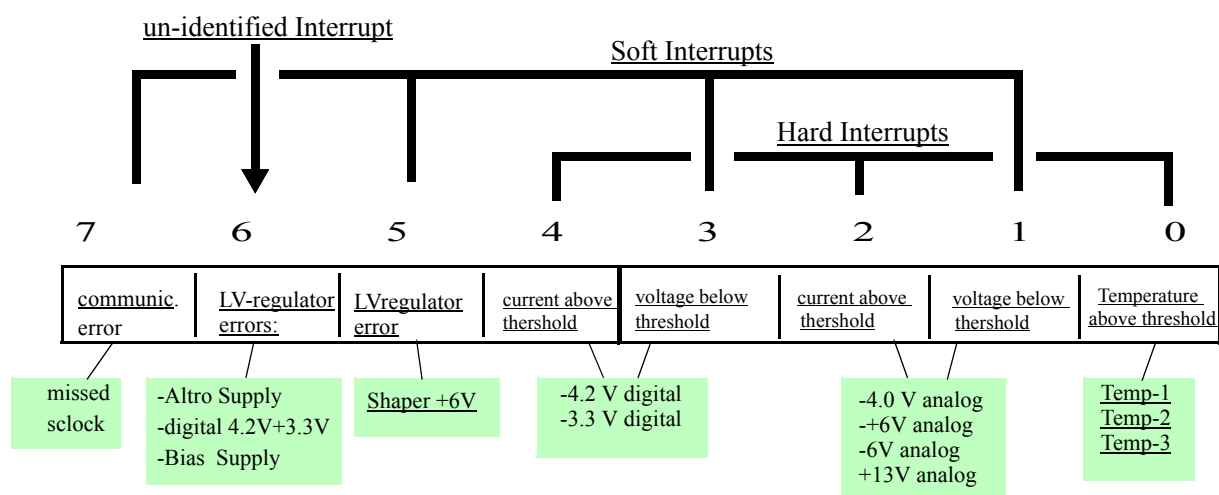


Figure 116 Sources for PHOS FEE interrupts

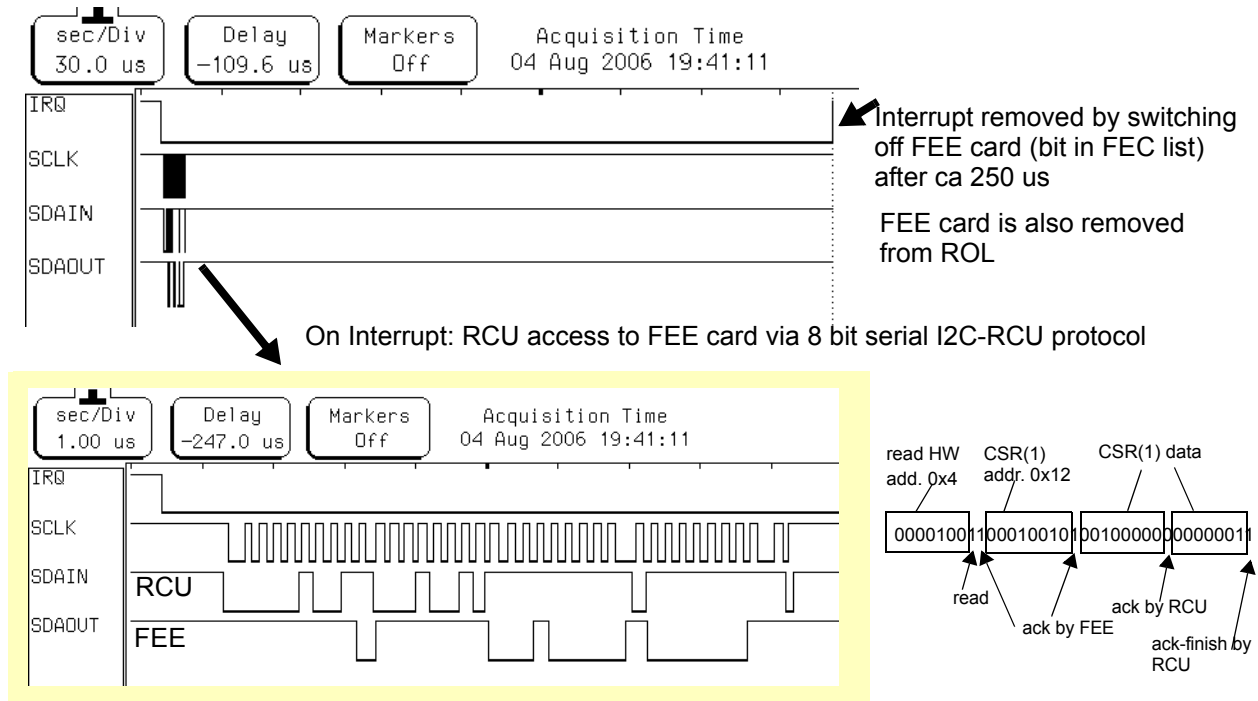
The Flag bits corresponding to error types as in Figure 116 are set by the PCM in the lower byte of CSR(1) at address 0x12 and in more detail in the PCM auxiliary register 0x65. When the RCU receives the interrupt and INTmode register is enabled to serve interrupts, the RCU starts scanning all those FEE cards which are enabled in the FEC list (0x8000) via the serial RCU protocol. The scan reads the CSR(1) at 0x12 of each FEE card and if it's interrupt bit (No 13) is set, it determines the type of interrupt from the pattern of bit <7..0> according Figure 116.

There are 3 types of Interrupts

1. Soft error: The PCM has discovered one of the sources for soft errors specified in Figure 116, it sets the “convert” bit in CSR(0) to non-automatic (0x01) in order to freeze the measurements taken by the AD7417. On receipt of the Interrupt, the RCU reads CSR(1) and disables in CSR(0) the corresponding mask bit which removes the interrupt from the bus. The RCU removes the FEE from the ROL at 0x8001 but not from the FEC list at 0x8000.
2. Hard error: The PCM has discovered one of the sources for hard errors specified in Figure 116, On receipt of the Interrupt, the RCU reads CSR(1) and when it identifies a hard interrupt, it removes the FEE from the ROL at 0x8001 and from the FEC list at 0x8000. This effectively switches off the FEE card.
3. Hardware error: The PCM has discovered one of the sources for soft or hard errors specified in Figure 116. On receipt of the Interrupt, the RCU tries to read CSR(1) but this is not successful. The RCU removes the FEE from the ROL at 0x8001 but not from the FEC list at 0x8000 and marks this situation in bit 8 of the Interrupt status memory.

The details of a hard and soft error as they are handled by the RCU serial protocol are depicted in

Hard Interrupt:



Soft Interrupt:

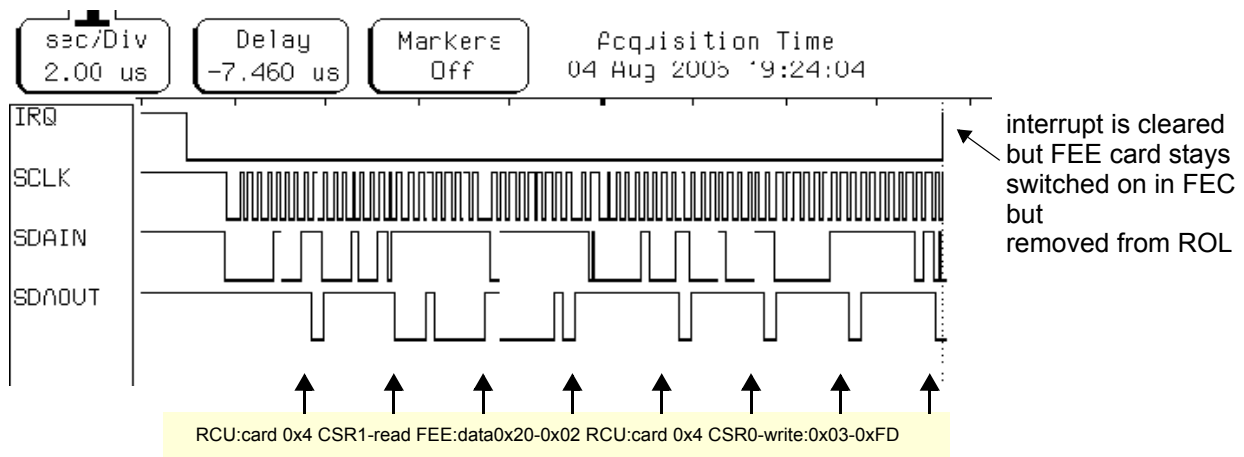


Figure 117 Top: RCU handling of a hard interrupt from FEE 0x4 (AD7417 temperature excess) Bottom: soft interrupt from FEE 0x4 (Voltage below threshold)

Note: In all cases the CSR(1), the PCM auxiliary Interrupt register 0x65 is to be read by the RCU for full decoding the reason of interrupt. The information is to be made available to the DCS system in order to notify the users to take appropriate action.

The CSR(0) at address 0x11 contains the 8 bit interrupt mask in its lower byte. Bit 10 is the AD7417 convert mode "cnv" which is set 1 for explicit conversion when the STCVN command (address 0x1b) is sent. When cnv is set to zero, the conversion is performed automatically by the AD7417.

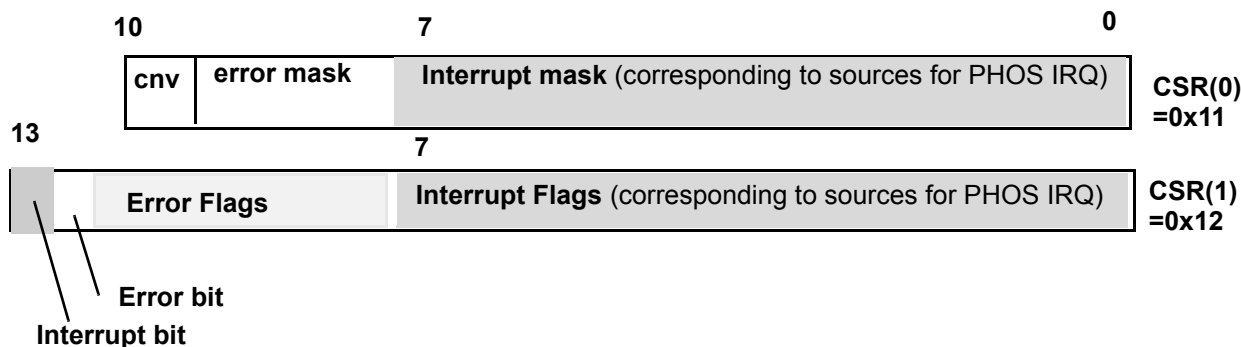


Figure 118 CSR(0) Error and Interrupt mask CSR(1) Error and Interrupt Flags

An example for reading values of status register CSR0,CSR1 is shown:

```

executing: w 0x7000 0x524011      # read CSR(0)
executing: w 0x7001 0x524012      # read CSR(1)
executing: w 0x7004 0x390000
executing: wait 1 us
executing: w 0x0 0x0
executing: wait 1 us
executing: r 0x7800
0x7800: 0
executing: r 0x6000 2
0x6000: 0x7ff 0                  # CSR(0)= 0x7ff CSR(1)= 0

```

The value 0x7ff of CSR0 means temperatures, voltages,currents updated continuously and mask all errors. The value 0x0 of CSR1 means that not a single error or interrupt is present

The PHOS FEE have more supply voltages and more temperature sensors than the TPC FEC. In order to allow the DCS to know also the sources of interrupts which are not contained within the mapping of the CSR registers defined for the RCU handling of the TPC, the PCM contains an auxiliary interrupt flag register at address 0x65 (see Figure 119).

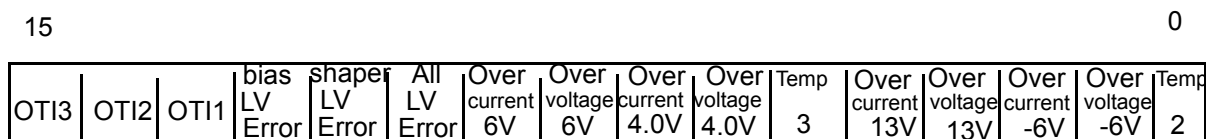


Figure 119 PHOS auxiliary Interrupt Flag register 0x65

The interrupt status memory (ISM) of the RCU is a block of 32 words of which the first word contains the

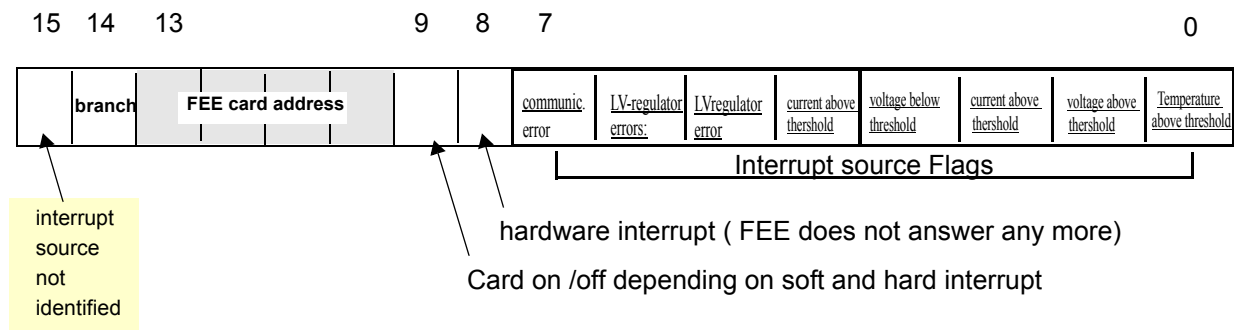


Figure 120 Format of interrupt status memory (32x16 bit words @ 0x 8100)

number of interrupt entries. By scanning the FEE cards after an interrupt the RCU places the information obtained from the FEE cards into the consecutive words of the ISM. If only the top bit is set (0x8000) it is an interrupt of which the RCU was unable to determine the cause (spurious interrupt, FEE card scan not successful etc). In case when bit 8 is set, the FEE card was identified but obviously has a hardware problem. In case of a hard error, the card was switched off in both FEC and ROL and this situation is indicated in bit 9. In all other cases, the branch and FEE card geographical address is indicated in the field <14:10> with the interrupt source flags as defined in Figure 116 contained in the bit field <7:0>.

The interrupt status memory can be cleared as follows:

```
enter operation (h/i/q/r/w): w 0x8100 32 0x0          #clear interrupt status memory
```

The CSR1 Flag register can be cleared by writing to PCM address 0x18

15.6 Error handling

The following errors can occur and lead to setting of error flags in the bit field < 11:8> of CSR(1) as defined in

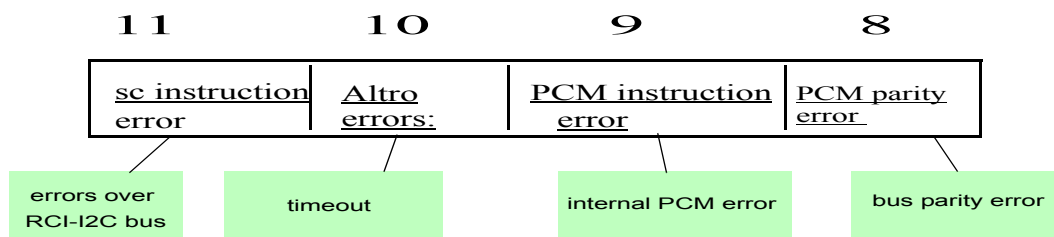


Figure 121 Sources of PHOS FEE errors

Figure 121. The bits 9 and 8 can be masked via the corresponding error mask bits 9 and 8 in the CSR(0). the bits 11 and 10 always lead to setting the error bit 12 in CSR(1) and the error line on the GTL bus is asserted.

15.7 Serial Interface for slow controls communication between PCM-RCU

The serial communication interface between the RCU master and the FEE cards serves for independent

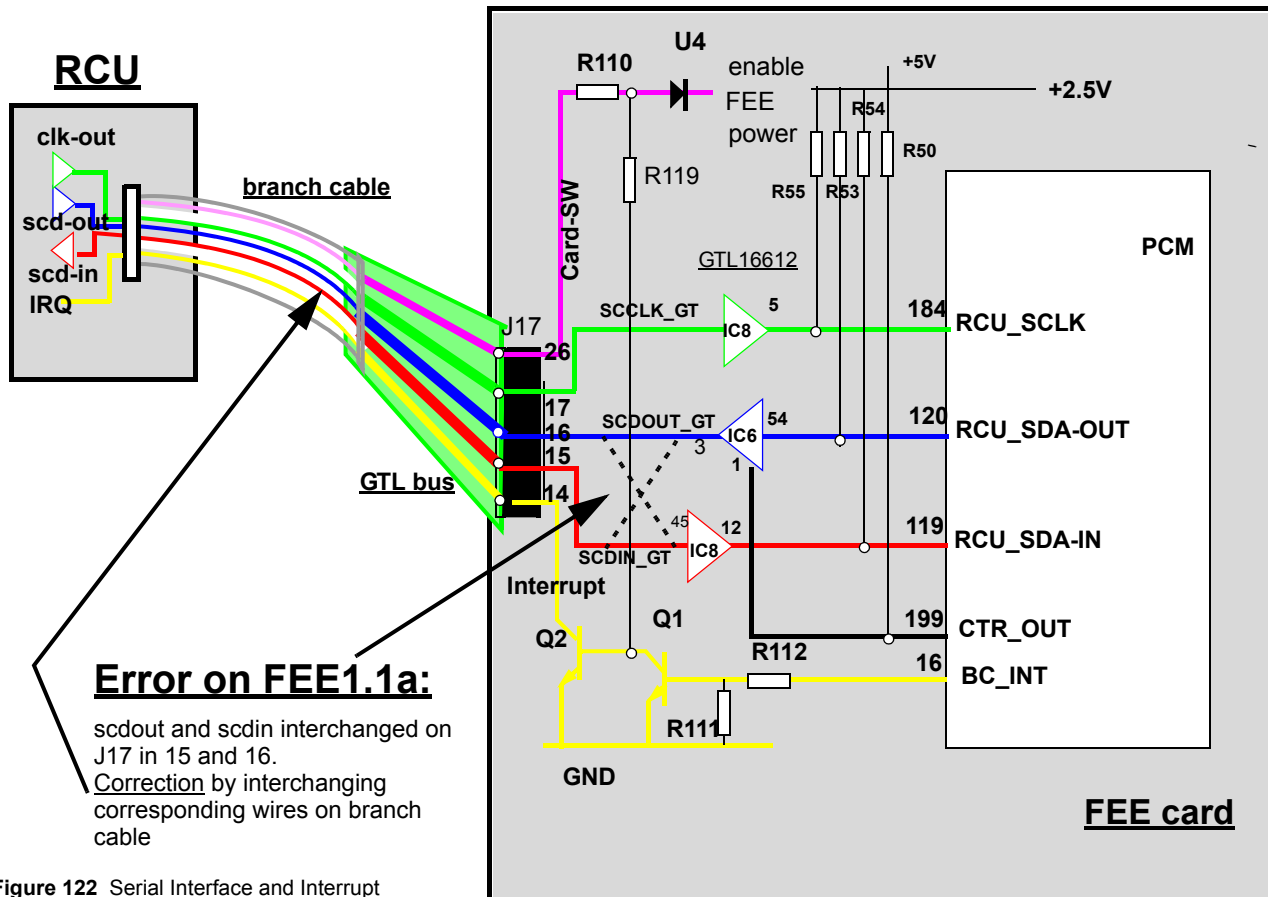


Figure 122 Serial Interface and Interrupt

communication during data taking and in particular for interrupt handling. Together with the Interrupt and Error lines driven by the PCM, the serial protocol belongs to the RCU **Safety and Monitoring** module.

The schematics of the serial interface between RCU and FEE cards is depicted in Figure 122. Unlike the bidirectional I2C the RCU serial protocol is implemented over two unidirectional signals RCU_SDA-IN and RCU_SDA-out with a common clock signal RCU_SCLK driven by the RCU master.

Note: on FEE card V1.1a and previous, the serial protocol out and in lines are inverted by error (see Figure 122) A remedy is the inversion of these 2 adjacent lines on the RCU branch cables.

In addition to the parallel bus, an I2C-like serial control network is mastered by the RCU via the SCDin and

Serial RCU protocol

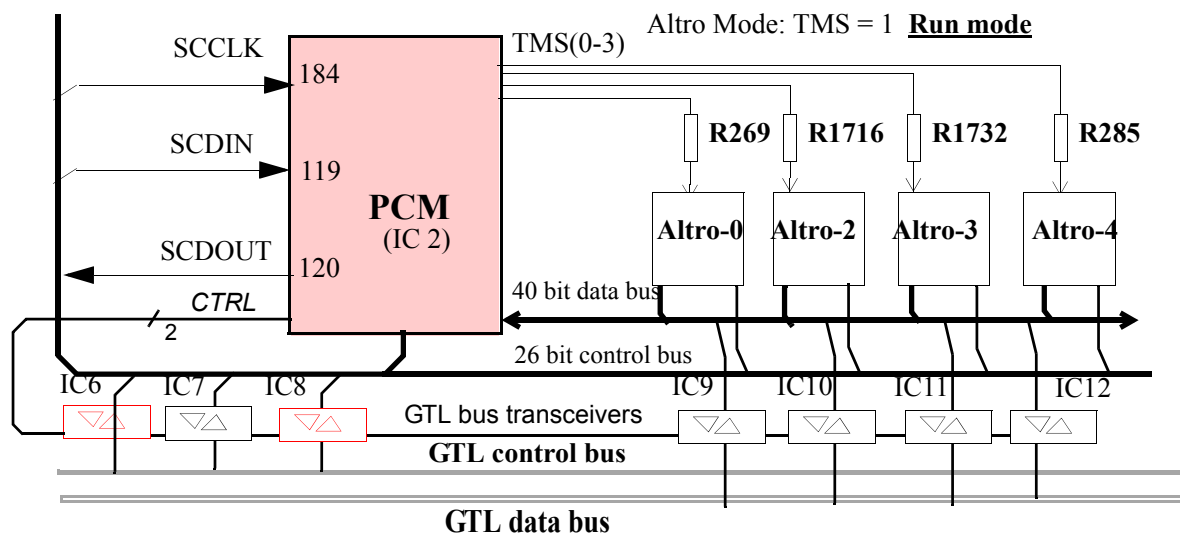


Figure 123 RCU -PCM serial network protocol overview

SCDout lines on the GTL control bus handled via the GTL bus trenceivers IC6 and IC8 (see Figure 123. This protocol is handled by the PCM as slave.

For PHOS, an extension of the TPC RCU serial protocol from 5 to 8 bit was required. The 8 bit SCadd register is depicted in Figure 124.

The serial interface is full independent of the normal data bus activity. This is particularly important for serving high priority interrupts whilst the data bus is busy. There are two important 16 bit registers which are however restricted to address 8 bit

SCadd -address field for serial interface 0x8005

SCdata -data field for serial interface	0x8006
---	--------

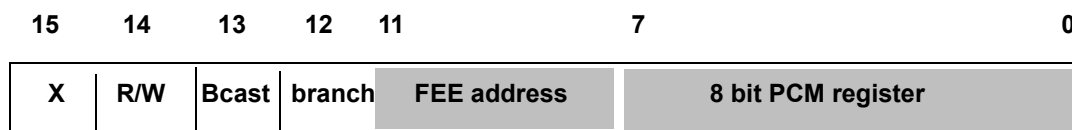


Figure 124 Seral command 8 bit address format of SCadd register

Example for access to PCM registers via serial interface:

w 0x8005 0x0111

```
# write CSR(0) at FEE 0x1
```

```

w 0x8006 0x0030      # write data 0x30
w 0x8010 0x0         # execute

w 0x8005 0x4111      # read CSR(0) at FEE 0x1
w 0x8010 0x0         # execute
r 0x8002              # read result register

```

Screenshots of the serial protocol during interrupt handling are shown in Figure 117

15.8 Altro Test mode

The CSR(2) register of the PCM is available on each FEE card for exceptional Altro hardware testing and debugging including enabling / disabling of clocks and power regulators.

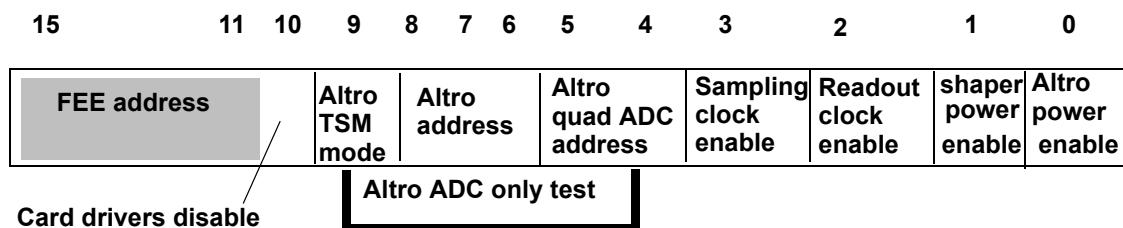


Figure 125 Test mode configuration register CSR(2)

Altro chips can in principle be used in 2 modes: Run mode and test mode, as defined by the TSM signal from the PCM (Figure 123), enabled via the Altro test mode of CSR(2). The test mode uses quad groups of Altro-internal ADC's directly, i.e. without using the Multievent buffer. The test mode was never required for PHOS testin therefore TMS signals are by default always high.

The "card enabling" bit removes any communication between RCU and FEE card and only allows for external reset or incoming commands via the serial interface. The sampling and readout clocks of the RCU are maintained when the card is disabled.

The lower 4 bits allow for specific tests with disabled clocks and power for the shapers and the Altro.

16 High Voltage APD bias control

The 32 APD's belonging to one FEE card are individually biased via 32 HV bias controllers on the FEE card and alimented from a common HV input of +400 Volt. All these HV inputs of FEE cards of one RCU branch are daisy chained via 0.5 ns Lemo cables on the FEE cards (see Figure 126 below)

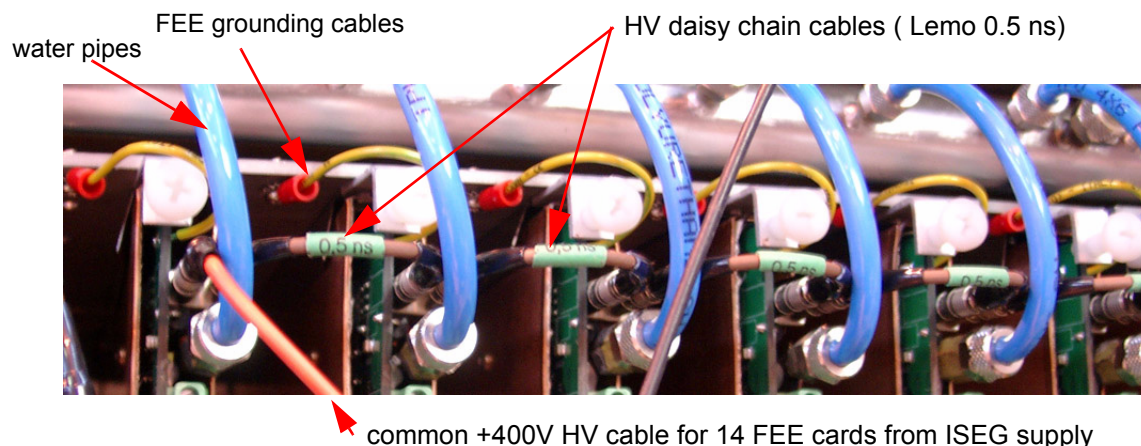
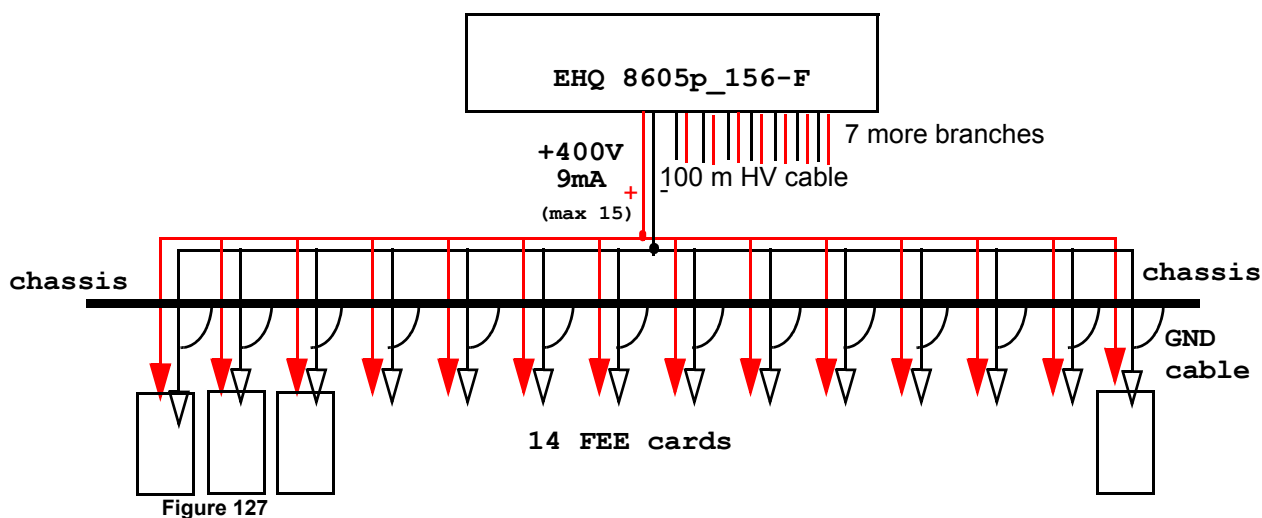


Figure 126 HV daisy chain and grounding cables of PHOS

The current to be supplied by the HV power supply for one daisy chained branch of 14 FEE is max. 9 mA. PHOS has chosen 8ctal power supplies from ISEG **EHQ 8605p_156-F** with 8 differential (floating) HV channels of max. 15 mA each. This allows for setting a convenient trip current limit between 10-15 mA.

The safety grounding of each individual FEE card is depicted as well in Figure 126. Short ground cables are soldered on one side to the ground point of the FEE card next to the HV Lemo connector, all these cables are connected to the common metallic frame of the FEE card guidance.



The HV connection from the dual LEMO input connector on the FEE cards is connected to the 32 -fold bias logic on the far left and right sides of the FEE card (see Figure 128 below). This left-right connection is implemented via an isolated wire (to avoid leakage currents on the PCB)

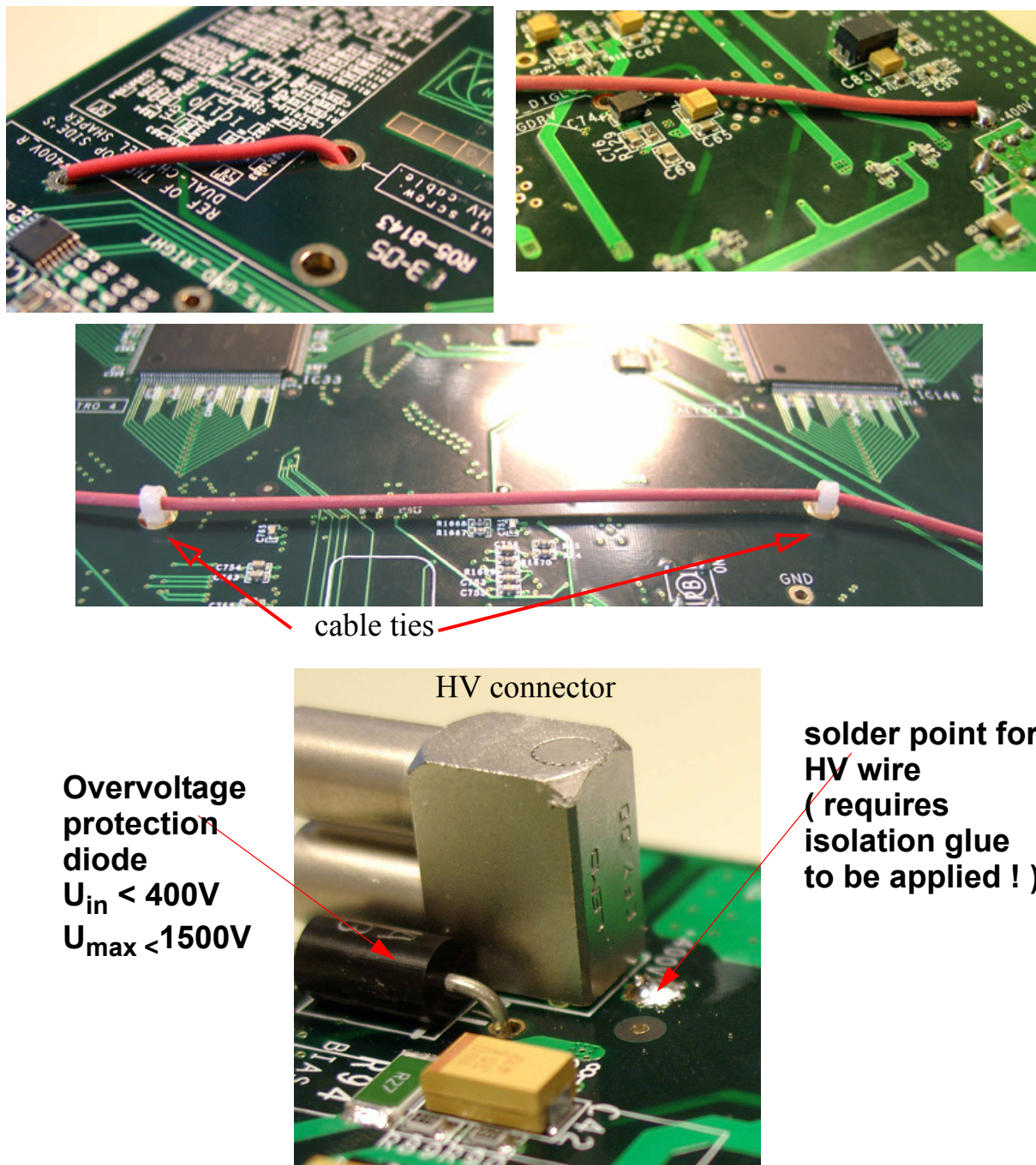


Figure 128 Details of the high Voltage distribution

Note: Do not use any other holes than the assigned ones for passing the cables as shown in Figure 128!

The photos of Figure 128 show mounting details of the High Voltage wire.

The input bias voltage should not overpass 400 Volt. The bias regulator logic (see optocouplers see Figure 139) is only protected by a protection diode and a 15 nF capacitor which clips Voltages above 400 Volt .

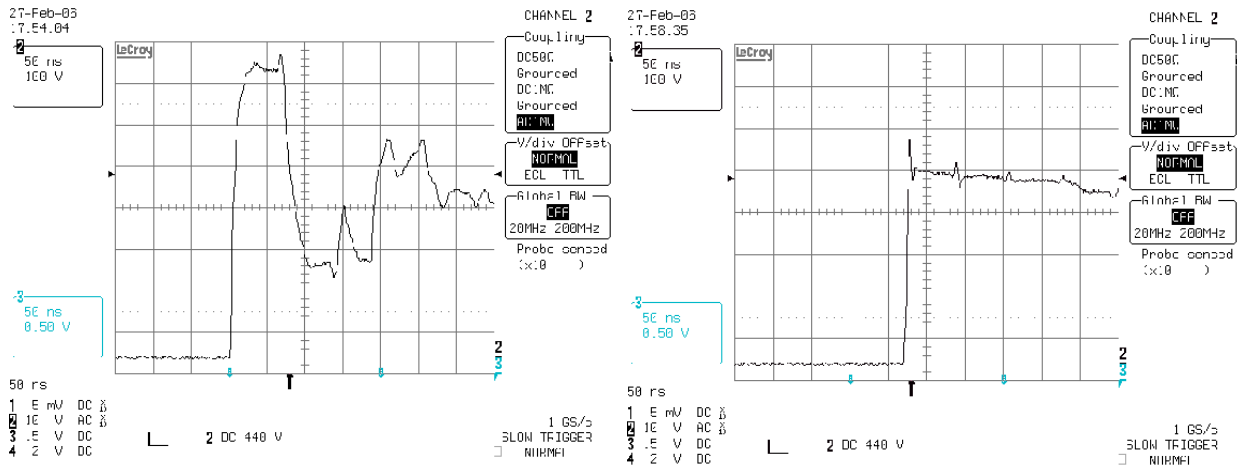


Figure 129 left side: Overshoot of High Voltage (400 Volt) without protecting diode at the FEE in case of disconnection / reconnection of HV cable at the HV supply . **right side:** same situation but with protection diode on the FEE card.

Due to the protection diode, overvoltage transitions due to hazardous HV cable-disconnection and reconnection (see Figure 129 (left)) are largely filtered by the protection diode of type 1.5KE-400CA. Figure 129 (right) shows the clipped overvoltage when the diode is installed, i.e the diode protects the FEE cards very efficiently from hazardous overvoltages.

Note : It is strictly forbidden to disconnect HV cables when HV is connected via long cables to the FEE cards ! First the voltage must be ramped down.

The bias voltage on the APD's is programmed via PCM registers as listed in Table 9. After a FEE reset, the PCM should reset all APD bias Voltages to a common, low value.

16.1 High Voltage distribution

The ISEG HV modules[7] are available in 6U Eurocard standard, with a single multi-wire Ernie connector for 8 differential HV channels. The EHQ 8405p_156F module has 8 * (500 Volt/15 mA) floating Ground HV connections (Figure 130) .

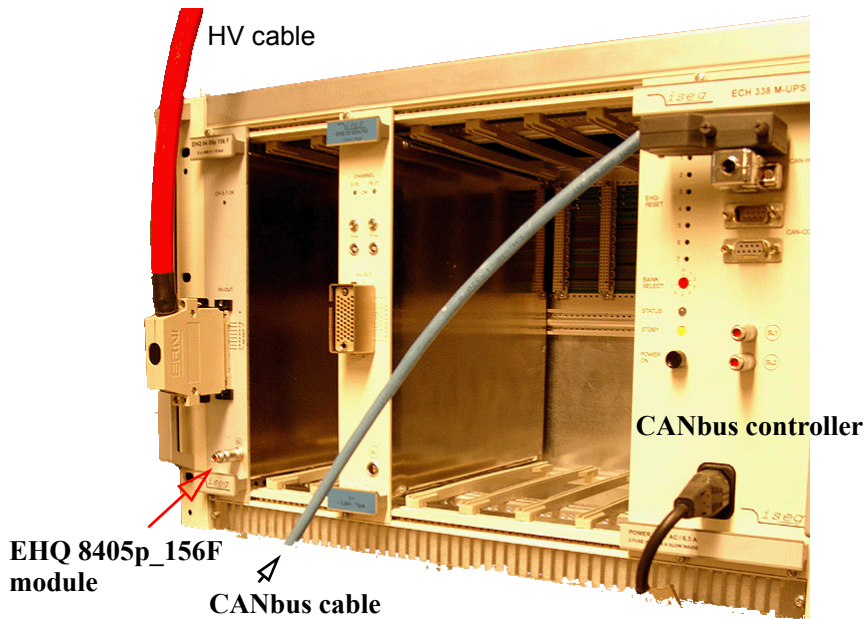


Figure 130 Iseg 6U HV crate with CANbus controller (right side) and 500 Volt EHQ module with ERNIE connector and cable (left side)

The HV connector provides 8 floating HV supply voltages to a multi-conductor HV cable ending up on a close-by HV patch panel with Ernie connectors (Figure 131) which serves as HV fan-in for three 37 wire HV cables of ca 100 m lenght which ends at the PHOS-HV patch panel in UX25 close to the PHOS detector. Each pair of the 37 wire cable contains 18 differential HV cables (plus one chassis ground).

At the corresponding patch panel in UX25, the 5 supply cables are de-multiplexed into their original 5 connectors corresponding to the ISEG modules in CR4. Each HV supply connector is connected to an octal splitter cable with standard coaxial crimping LEMO connectors of size 00 at each end. The positive wire of each HV pair is connected to the inner connector pin, the negative to the lemo chassis.

Each connector feeds one HV daisy chain of 14 FEE cards. One ISEG supply feeds therefore all eight RCU branches of the PHOS module. The nominal current for 14 FEE cards is 9 mA.

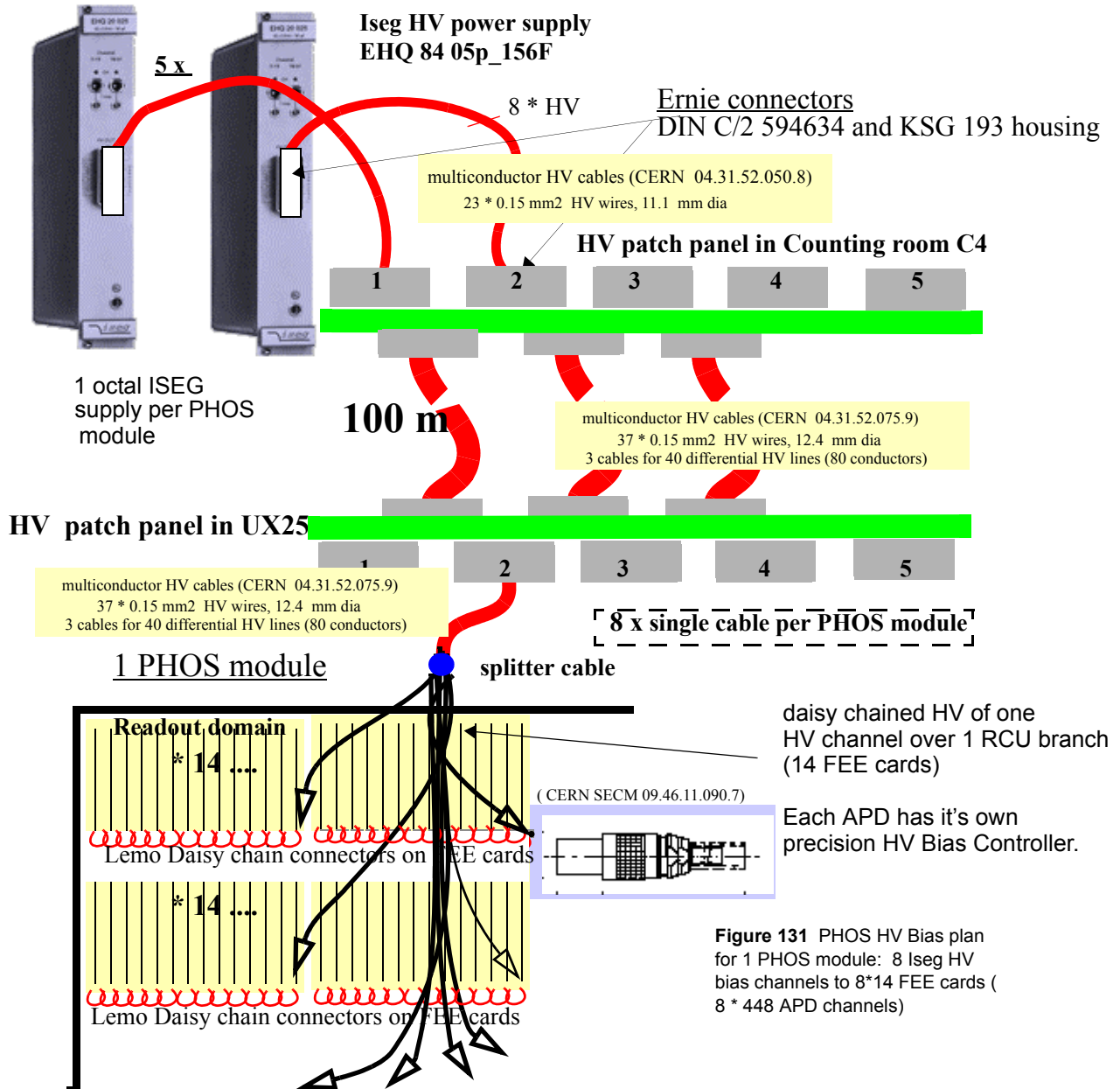


Figure 131 PHOS HV Bias plan for 1 PHOS module: 8 Iseg HV bias channels to 8*14 FEE cards (8 * 448 APD channels)

16.2 HV supply stability test

A single ISEG channel is daisy-chained to 14 Readout boards in the PHOS detector.

PHOS uses Avalanche Photo Diodes for scintillation light conversion. The APD's are operated in reverse mode at Voltages between 300..400 Volt, i.e. at very little leakage current (ca 1 nA). Each APD bias Voltage is regulated individually to obtain a charge gain of $M=50$. As a sideeffect of the regulation electronics, each APD channel requires more current, namely 20 μA per channel in order to keep the regulation loop stable.

Iseg HV Supplies in PHOS context

The Iseg HV supplies EHQ 8405p-156-F provide up to 500 Volt on 8 differential channels with floating grounds and each channel can deliver up to 15 mA with a precision of 2×10^{-4} . Due to the very high dependence of the APD gain on the Bias Voltage, PHOS requires a very high HV stability, also on the un-regulated bias voltage input.

The individual APD HV settings are controlled by high-precision bias controllers on the FEE cards which all receive the same HV input from the ISEG supply. RCU branches of 448 APD channels are fed by single Iseg EQH channels at an average current of 9 mA. The common input Voltage (400 Volt) allows the individual HV bias controllers to set APD bias voltages between 210 and 400 Vol with a precision of 0.2 Volt per set bit.

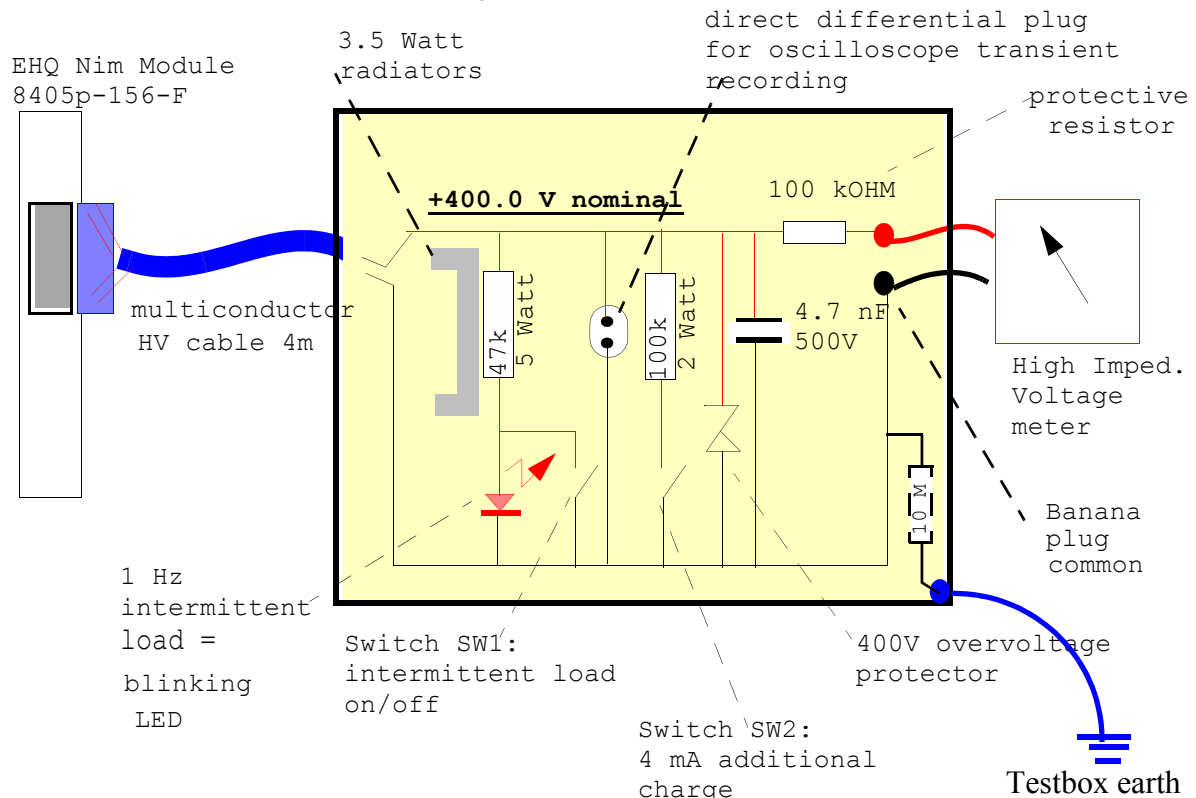


Figure 132 8 channel Test Box for emulating PHOS load situations

In order to investigate long-time and load dependence in the laboratory, a load test box has been built which replicates the PHOS Module nominal current consumption and provides for load tests with 2 different switchable current options and a intermittently pulsed current option for as a worst - tests. The test box (Figure 132) is connected over 4 m of HV multicore cable¹: on one side it connects to the ISEG HV connector on the other side it ends up inside the metallic testbox. The testbox replicates the current consumption of 1 complete PHOS module i.e. it consumes current on all 8 channels of one EHQ supply in parallel, equalling a nominal constant power conversion of $8 \times 3.5 \text{ Watt} = 28 \text{ Watt}$! Therefore the test box is a metallic box with

1. CERN SCEN code 04.31.52.075.9, CABLE HT 37*0.15 mm coaxial 3 KV

heat dissipators. The access points for measuring are both direct and protected: The direct access point for transient recording via a storage oscilloscope is a dual coaxial connector with protected pins. The 100 kOHM protected access for a precision Voltmeter is provided via eight Banana-plugs, one per HV channel. All these share a common, analog ground like in the PHOS electronics. (there is one Banana plug for the common ground). The metal test box has no connection with any of the positive or negative High Voltage lines. It must therefore be earthed in order to avoid static charging. An internal 20 M-Ohm between the common pole and the Chassis ground provides that static charging is limited.

Like in the FEE electronics, a bidirectional overvoltage protection diode clamps overvoltages above 400 Volt. A capacitor (4.7 nF) replaces an equivalent capacitance of 100 m supply cable.

There are 3 different test modes per channel depending on the choice of the two selection switches:

SW1,SW2=0,0 **constant load= 9 mA**

SW1,SW2=1,0 **intermittent load 9 mA pulses @ 1 Hz on/off**

SW1,SW2=0,1 **constant load= 13 mA**

SW1,SW2=1,1 **constant load 4 mA + intermittent load 9 mA @ 1 Hz on/off**

The test setup is depicted in Figure 133.

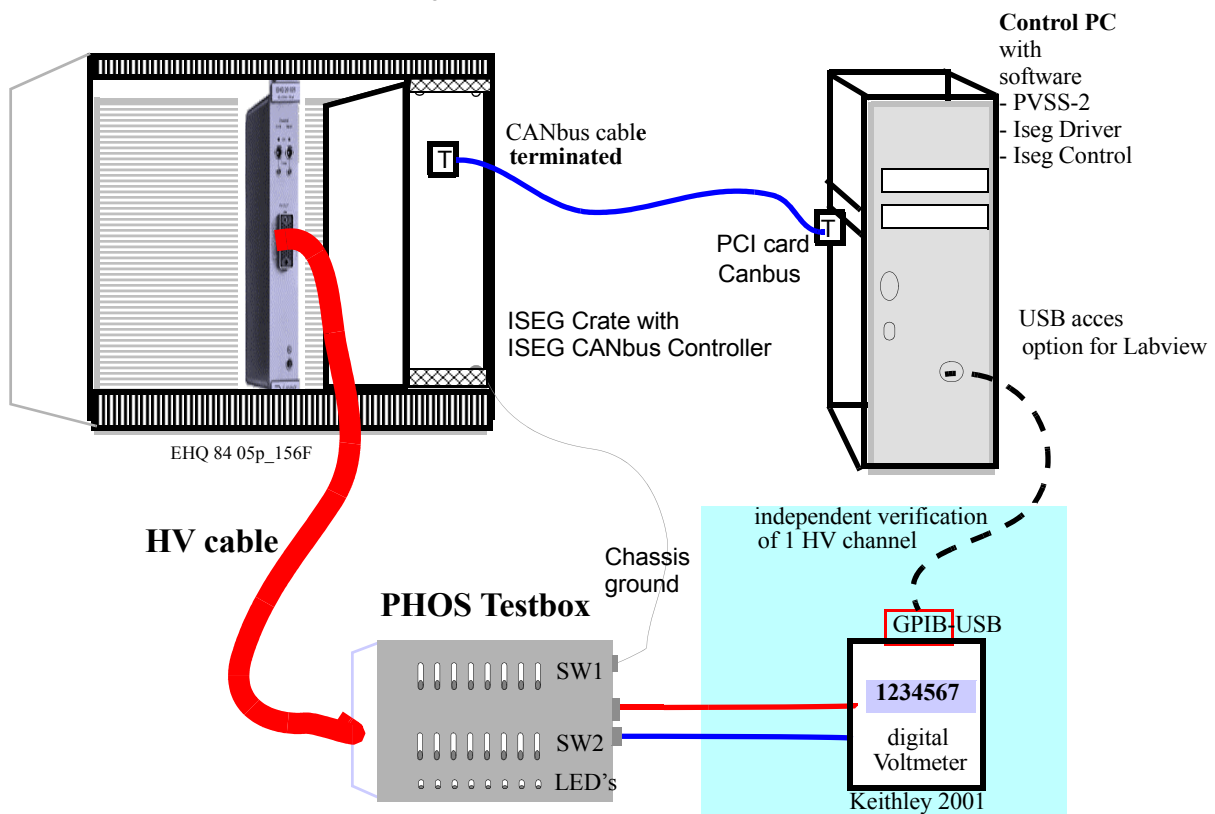


Figure 133 Laboratory Test environment

The ISEG software and hardware allows that both current and voltage settings are read back by software. An independent, high precision Voltmeter (6 digits Keithley 2001) allows that these readings are verified and if necessary calibrated.

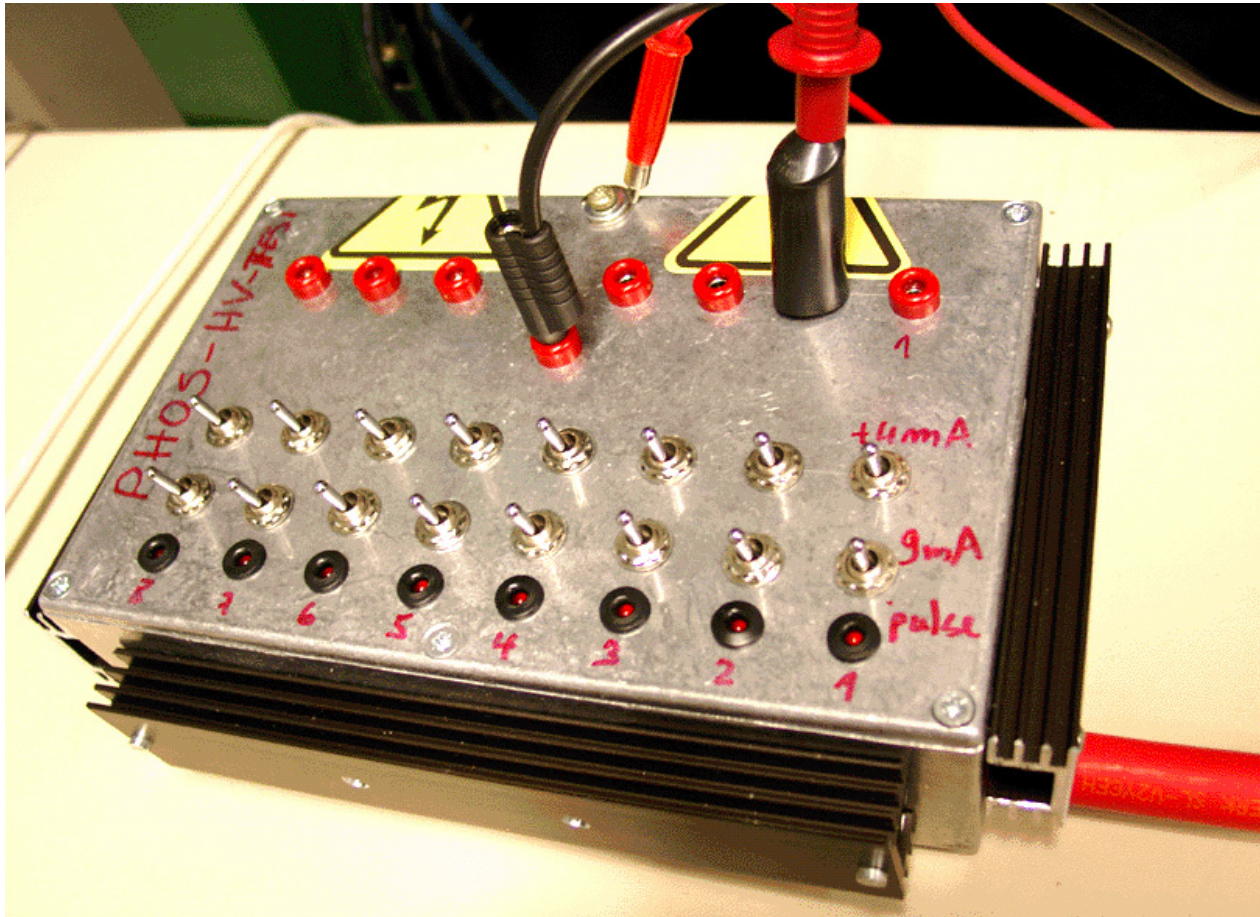


Figure 134 Photo of 8 channel PHOS testbox for equivalent load of 1 PHOS module

The Control screen of the Iseg HV software, which works via a CANbus to a PCAN-PCI card in the Control PC, is shown in Fig. 71. The ramping speed and trip current values are settable, and the real status of the HV output at the HV supply is shown. The current display in the test with the test load shows around 8 mA for 380 Volt. The status display for each channel shows (in green) an OK status which after a trip condition turns red.

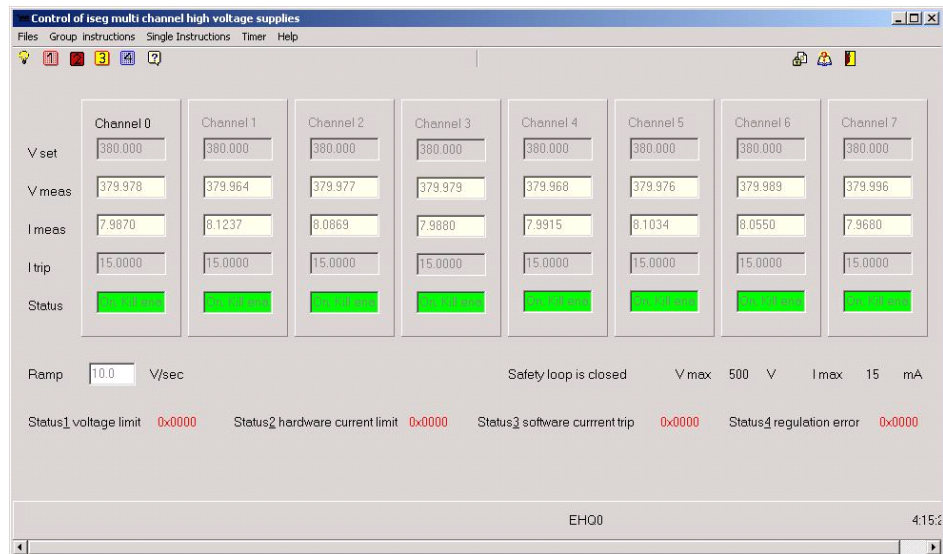


Figure 135 Control screen of lseg HV with status display for 8 channels

16.3 PVSS test of HV behaviour under load

Using the OPC server provided by ISEG, S.Popescu of DCS group has written a standard Control screen in the CERN PVSS language, which she used for testing OPC server stability and Alarm handling together in the

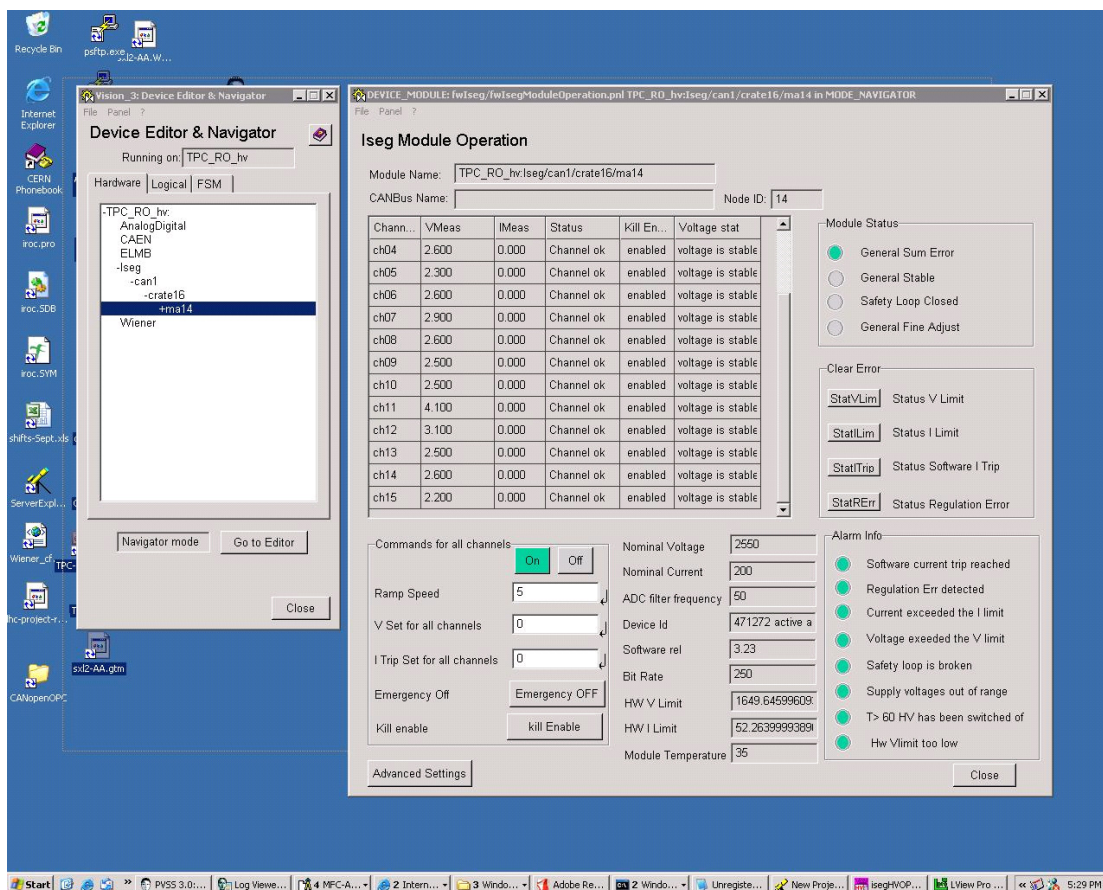


Figure 136 PVSS control screen for ISEG HV supply (written by S.Popescu)

Framework Fwiseg environment [25]. The ramping history plots of 4 Iseg HV channels are depicted in Figure 137.

The measured longtime load behavior of the Iseg EHQ 84 05p_156F module over CANbus / PCAN-PCI is shown Figure 138. The 4 channel stability test over 2 hours showed ± 0.01 V deviations over time and dynamic loads produced by the PHOS test box. At 380 V this corresponds to a HV stability of better than 10^{-4}

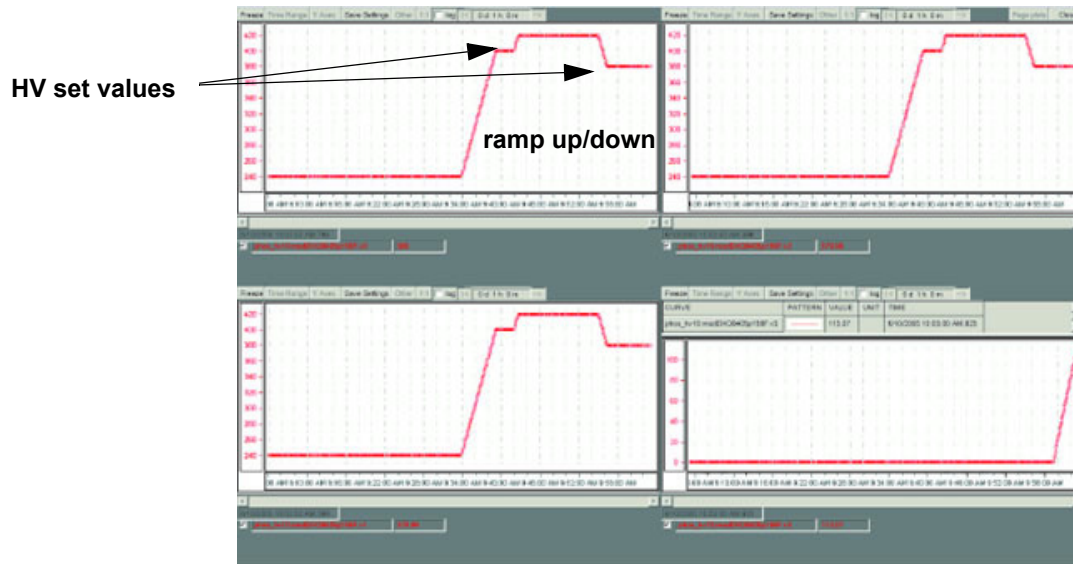


Figure 137 HV ramping history of 4 Iseg channels recorded in PVSS environment [25]

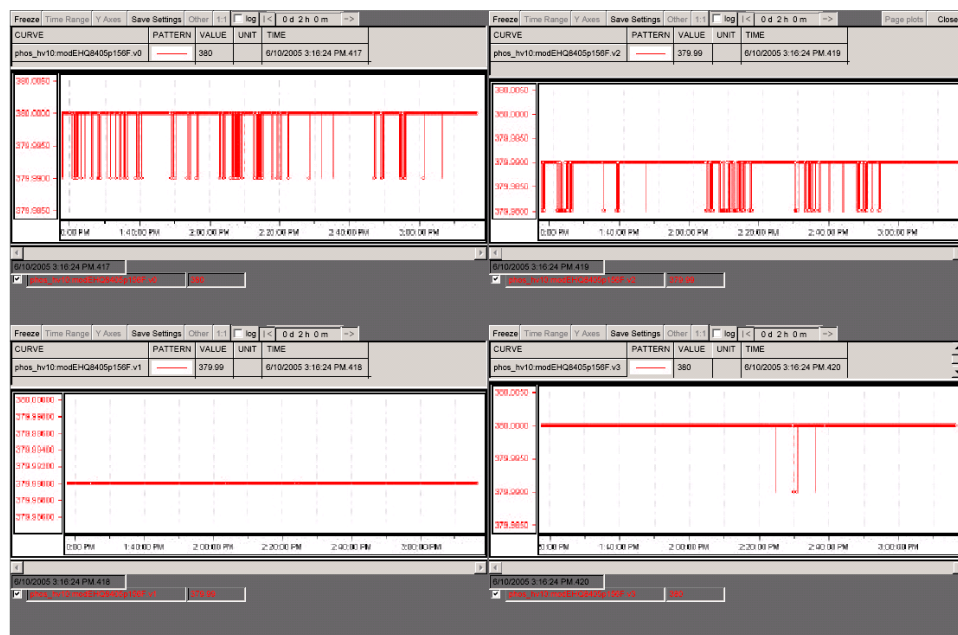


Figure 138 PVSS based Iseg Stability plot over 2 hours [25]

16.4 APD bias Voltage control [8]

There are 32 equal High Voltage controller circuits [20] on the FEE are grouped in two blocks of 16 on the left and the right side of the FEE board (compare Figure 70.) One individual HV block is shown in Figure 139., The

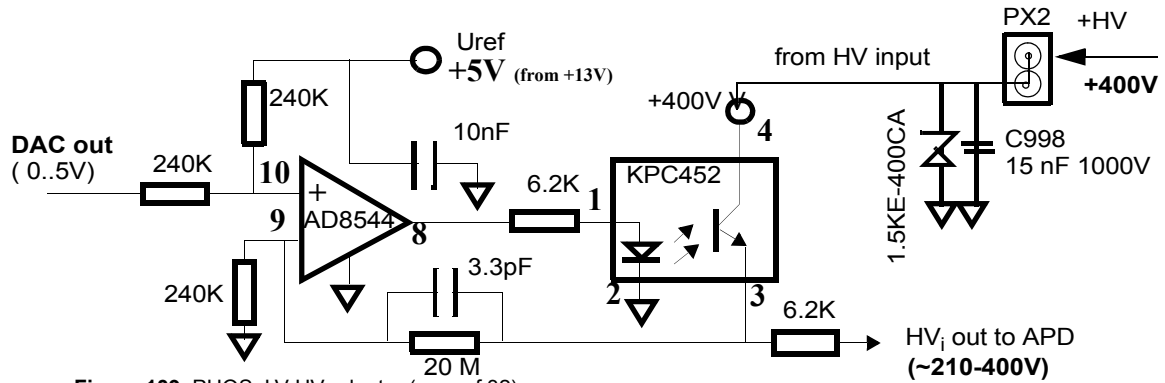


Figure 139 PHOS LV-HV adapter (one of 32)

programmable analogue DAC voltage generates with the +400V input a bias Voltage between a nominal range of 210 and 400Volt. Individual channels can have 210 +/- 5 Volt as minimal value.

A photo of one of the blocks with 16 HV controllers is shown in Figure 143. All KPC 452 optocouplers are connected to the same HV input (from dual LEMO connector) which has an HV input of max. 400 Volt The 1.5KE-400 Diode protects from overvoltages above 400 Volt. The linear relation between DAC setting and High voltage bias of an APD is shown in Figure 140

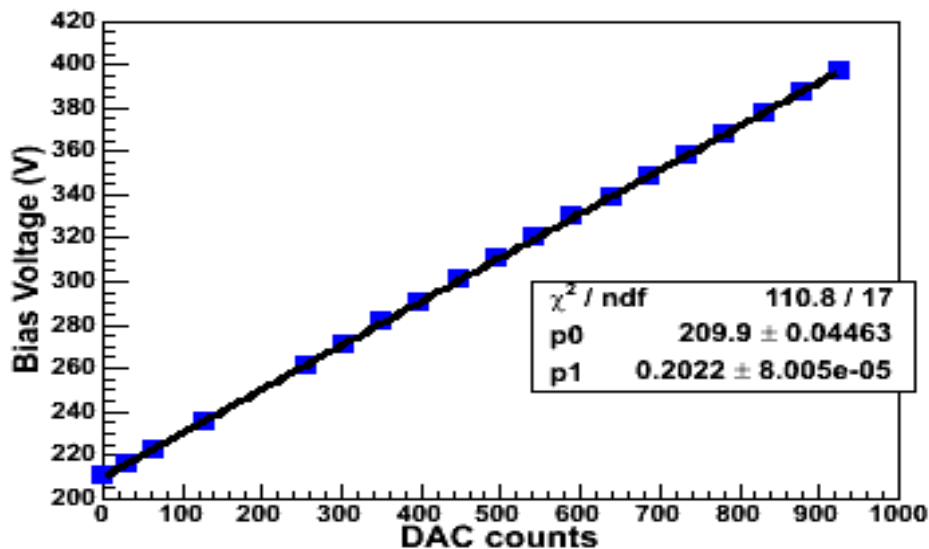


Figure 140 High Voltage versus DAQ

The nominal relation is

$$\text{Bias-Voltage[Volt]} = 209.9 + 0.2022 * \text{DAC count}$$

The software method for programming Bias Voltages and the mapping of register addresses to CSP channel numbers is detailed in Chapter 15. The pinout of the KPC optocoupler and of the octal DAC MAX 5304 is shown in Figure 141.

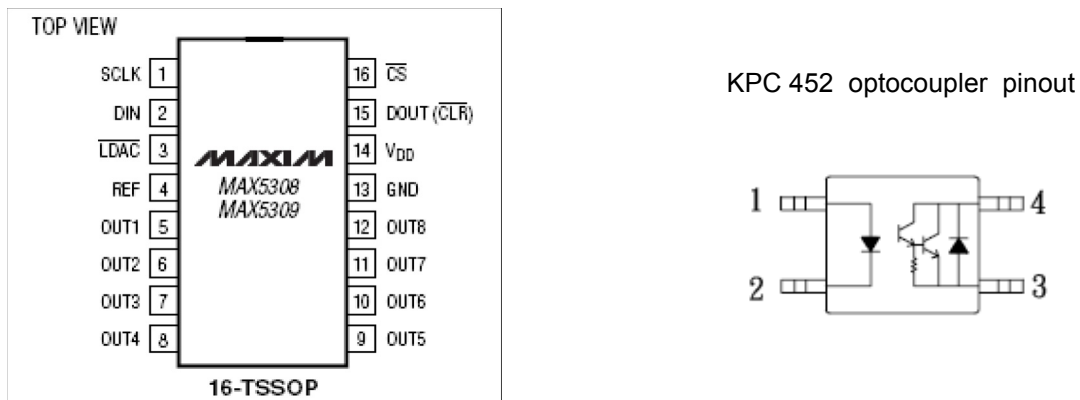


Figure 141 Pinout of octal DAC chip and of optocoupler in HV bias logic.

Note: defective optocouplers can be identified by programming the bias voltage low (210 Volt). If the voltage stays significantly above this value, the optocoupler's transistor is damaged and the optocoupler needs to be replaced. The low value HV values of all 32 channels may vary between 209 to 215 Volt, this is normal.

As shown in Figure 142 there are four blocks of 10 bit DAC's (octal DAC of type MAX 5304) under control of the PCM firmware. The SPI serial bus protocol (Motorola) is used by the PCM to load all DAC registers via the Din-Dout Daisy chain. The LDAC pin can be used to load all DAC's in parallel.

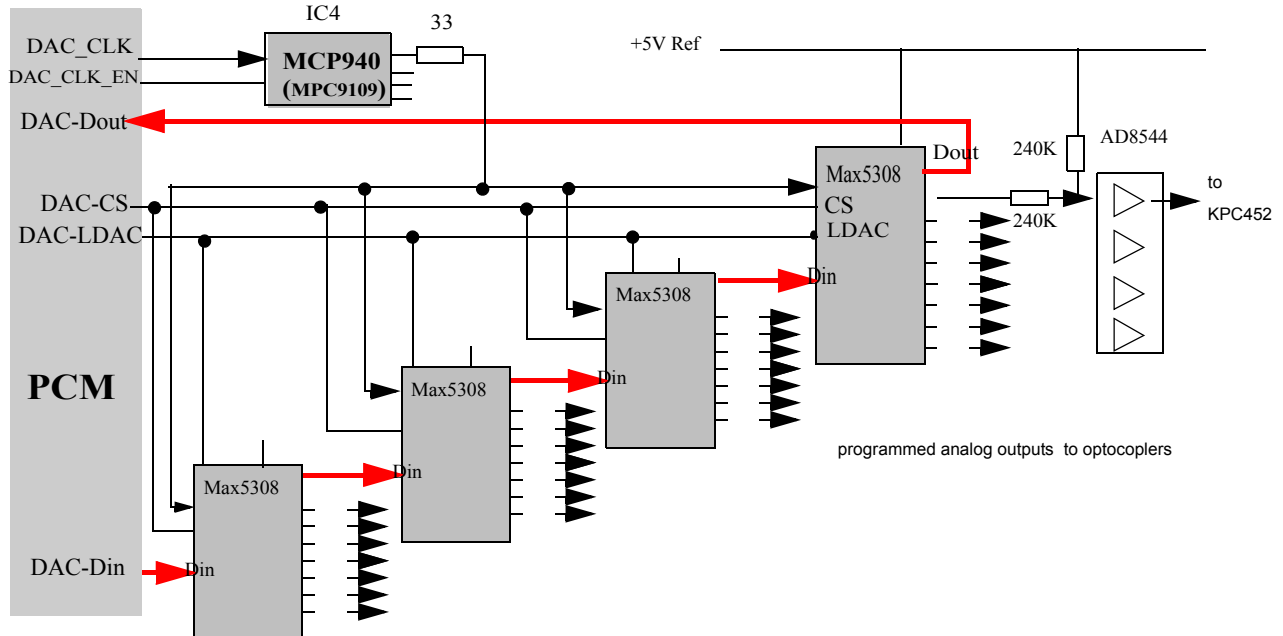
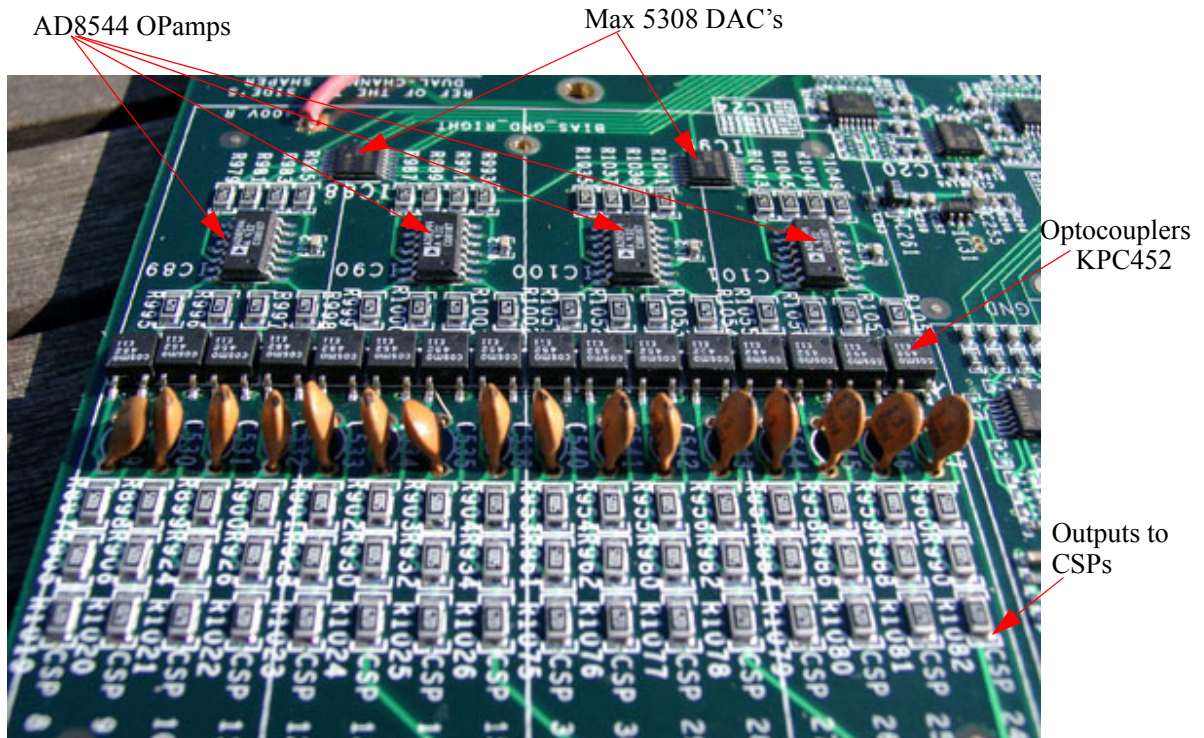


Figure 142 SPI serial bus control of the DAC controllers for the Bias Control blocks.



ATTENTION: dangerous High Voltage in this domain !!! For Laboratory work, cover this area via capton or some insulating foil or tape.

Figure 143 Photo of one 16-fold Bias Control block

16.5 Measuring the APD Bias Voltages

The bias voltages are programmed via the PCM register listed in Table 9. The programmed values can be read back from the 10 bit DAC, however these values do not necessarily represent the real bias voltage (in case of a defective optocoupler for example).

The real voltages can only be measured via a high ohmic a digital voltmeter. The probe positions for measuring

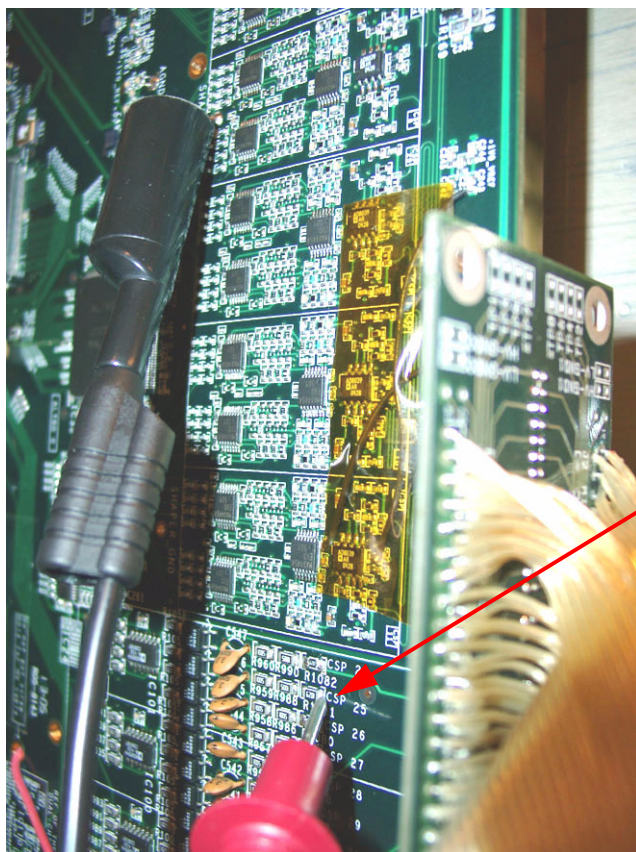


Figure 144 Measuring the Bias HV of individual CSP channels: Connect DVM to Ground pin (black probe top) and point with DVM probe tip to resistors marked as CSPx

High Voltage test points

the bias High Voltage for each CSP on the FEE card is shown in Figure 144. The Ground reference probe is connected to a wire tab at the analog ground. The positive probe is applied to the 6.8 K resistors next to the printed CSP numbers. If +400V input is applied, the minimal programmed voltage is ca 210 Volt and the maximum Voltage ca. 399 Volt¹.

The register addresses which correspond to the CSP numbers are listed in Table 9. See also Figure 143.

1. Note: symptom for a defective optocoupler is that the minimum Voltage 210 Volt cannot be programmed.

16.5.1 Measuring HV inside PHOS

Inside the PHOS cradle, the HV measuring points are only accessible on the IPCB via a long measuring probe. Such measurements may be needed if doubts about the defacto conversion of the DAC values arise.

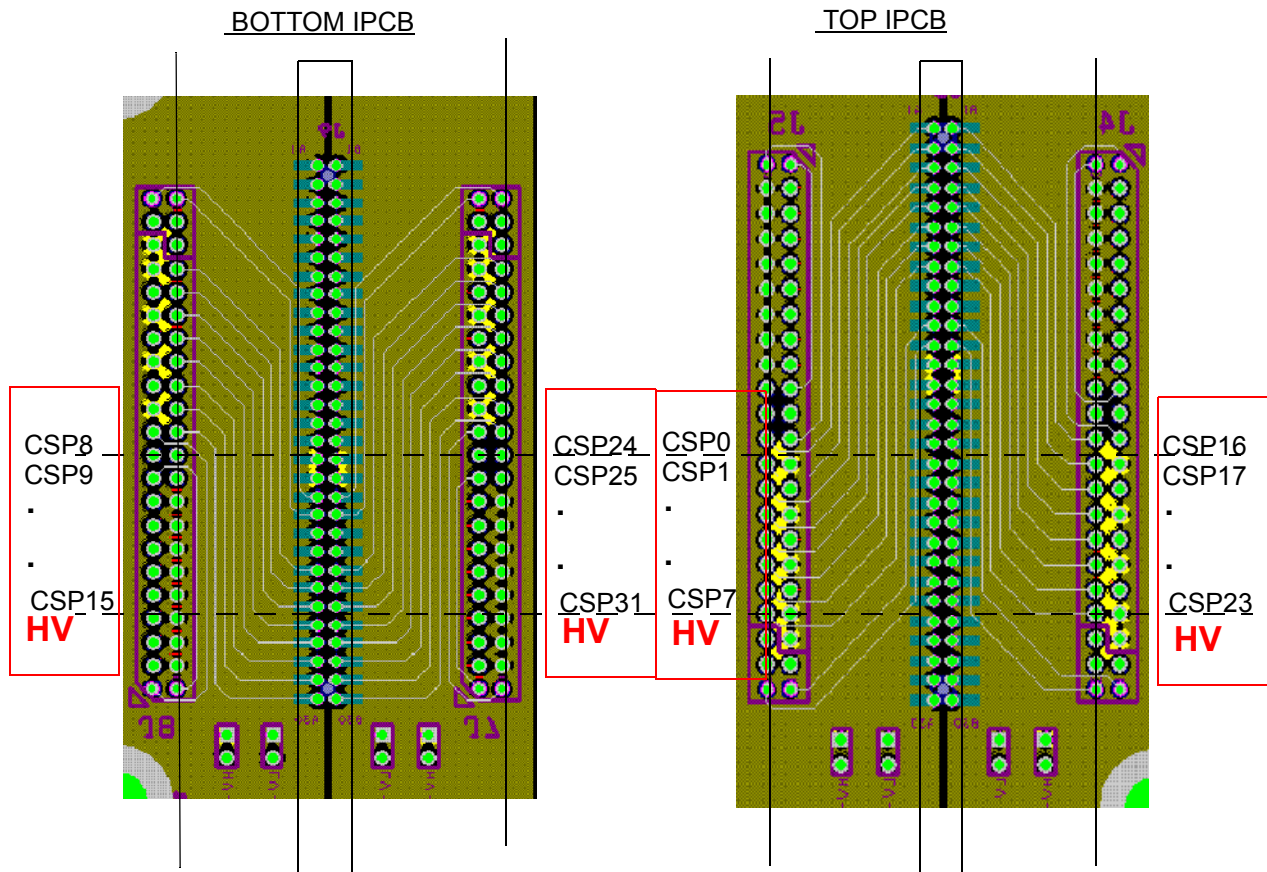


Figure 145 access to FEE signals on IPCB inside PHOS (as seen from FEE card side)

17 Analog reference Voltages

The correct reference voltage for shapers and ADC is very crucial for the correct data readout. Wrong reference voltages may result either in high pedestals, or signal cutoff.

The Altro Reference Voltage regulator is shown in **Figure 146**

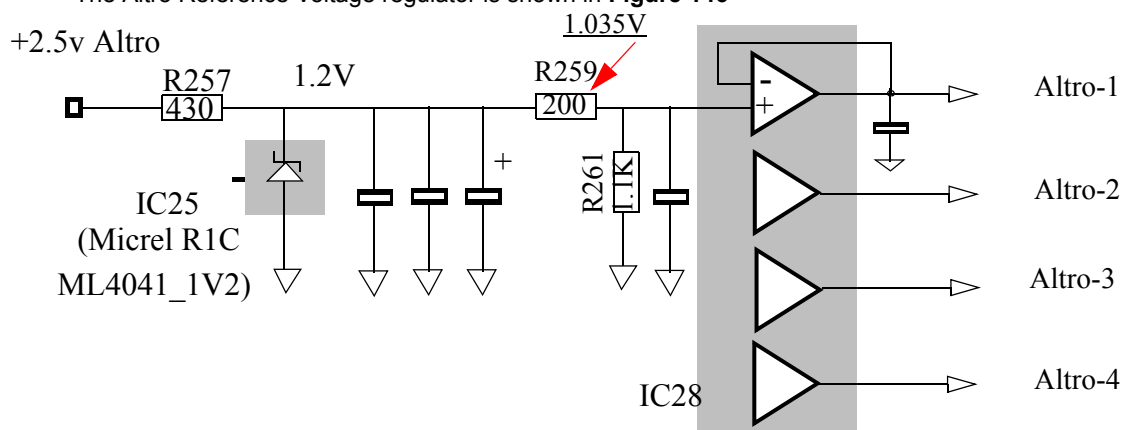


Figure 146 Altro Reference Voltage Generator

The high precision Reference Diode IC25 produces 1.2 Volt, the resistor divider reduces it to 1.035 Volt (corresponding to signal pedestals between 20 and 40 counts). The Resistor R259 produces a reference voltage of 1.035 Volt (see Figure 147).

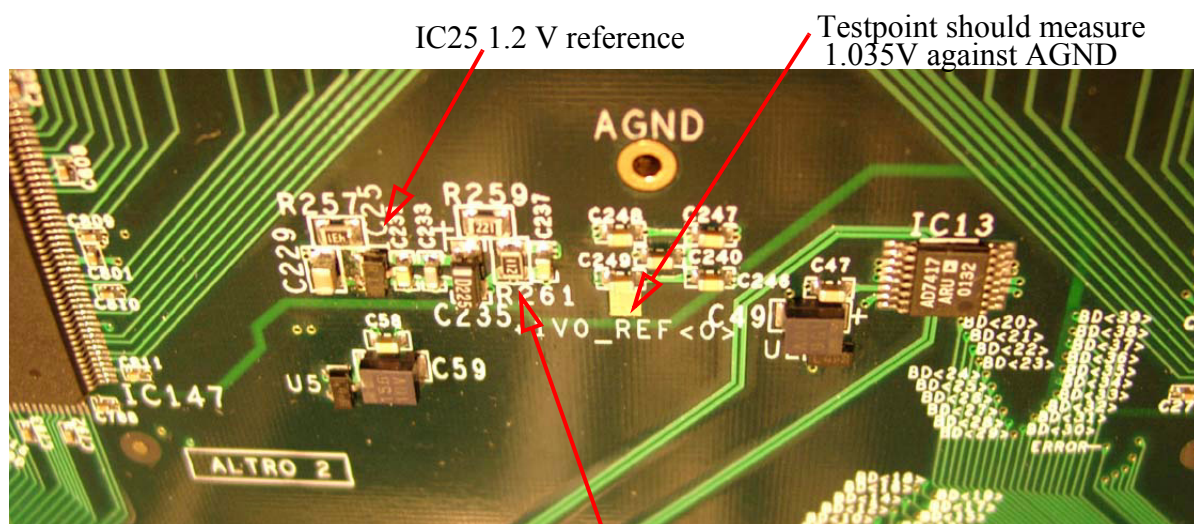
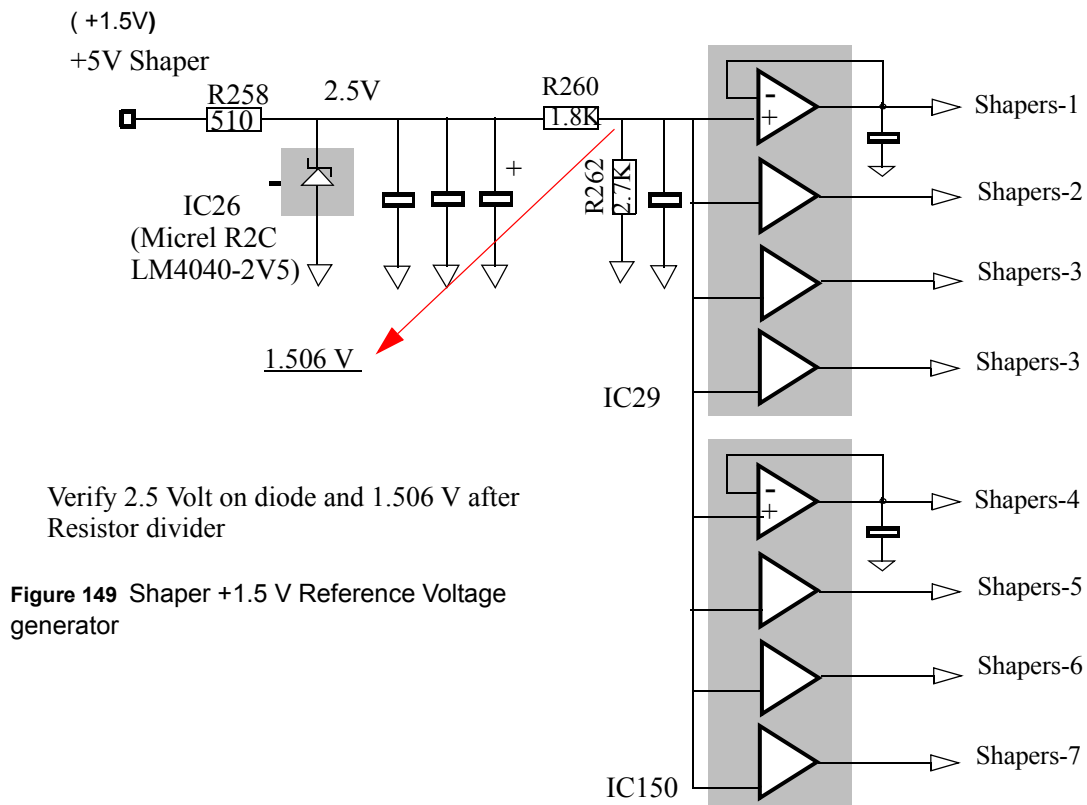
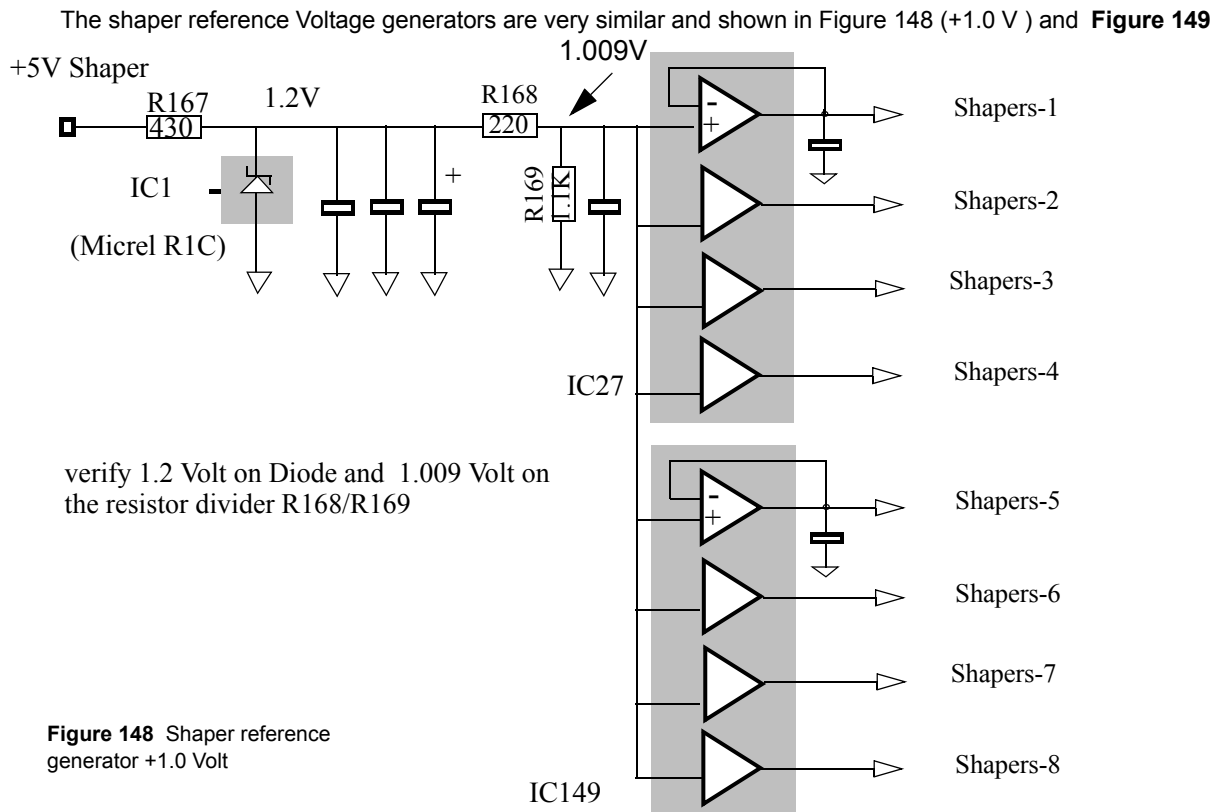


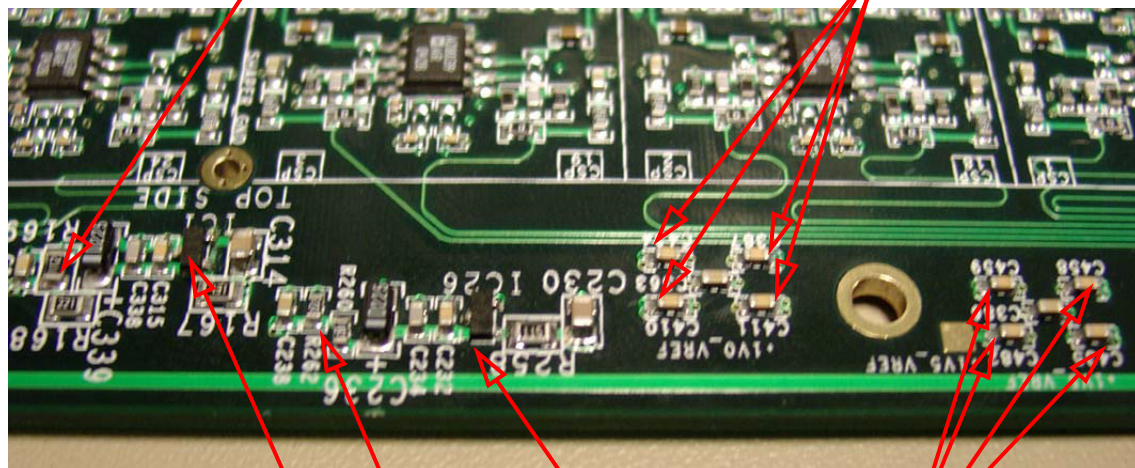
Figure 147 Photo of Altro Reference Generator



The component placement of the two shaper reference generators are shown in Figure 150

Resistor divider R 168/R169 from 1.2 Volt to 1.021V

testpoint +1V shapers 1,2,3,4



IC1 1.2 Volt reference

IC26 2.5 Volt Reference

Resistor divider R 260/R262 from 2.5 Volt to 1.5V

testpoint +1.5 V shapers 1,2,3,4

Figure 150 Photo of Shaper Reference Voltage generators 1.0 V and 1.5 V

The nominal reference voltage values for pedestals between 30 -40 counts (see Figure 40) are shown in Table 8:

Table 8: Reference Voltages

	Nominal	Remark
Altro	1.035V	can be tuned via R259/261
VREF 1.0	1.009V	can be tuned via R168/169
VREF 1.5	1.506V	can be tuned via R260/262

17.1 Readout and Sampling clock

The PCM slave logic is mastered by the parallel RCU/Altro bus and optionally also by the serial RCU protocol. Individual PCM registers can be addressed and commands can be executed by the RCU bus master with acknowledgement by the addressed PCM chip. DCS commands which address the Altro chips on the FEE card are acknowledged by the addressed Altro chips.

The RCU bus mastership can be switched to USB mastership [16] [10]. This functionality is however not yet fully available. The manual switch SW1 (Figure 158) allows to select mastership for the RCU (RUN mode =default) or for the USB (testmode).

In this document only **RUN mode with RCU master** is assumed. The 40 MHz readout and Altro sampling clocks (nominally 10 MHz¹) are selected by the SW1 switch. In RUN mode the Readout and Sampling clock are derived from the RCU's GTL bus. In TEST mode, these clocks are generated by the PCM. The measuring points for the sampling, readout and DAC clocks are shown in Figure 151. Note that all clocks are fanned out 4 times from a single source.

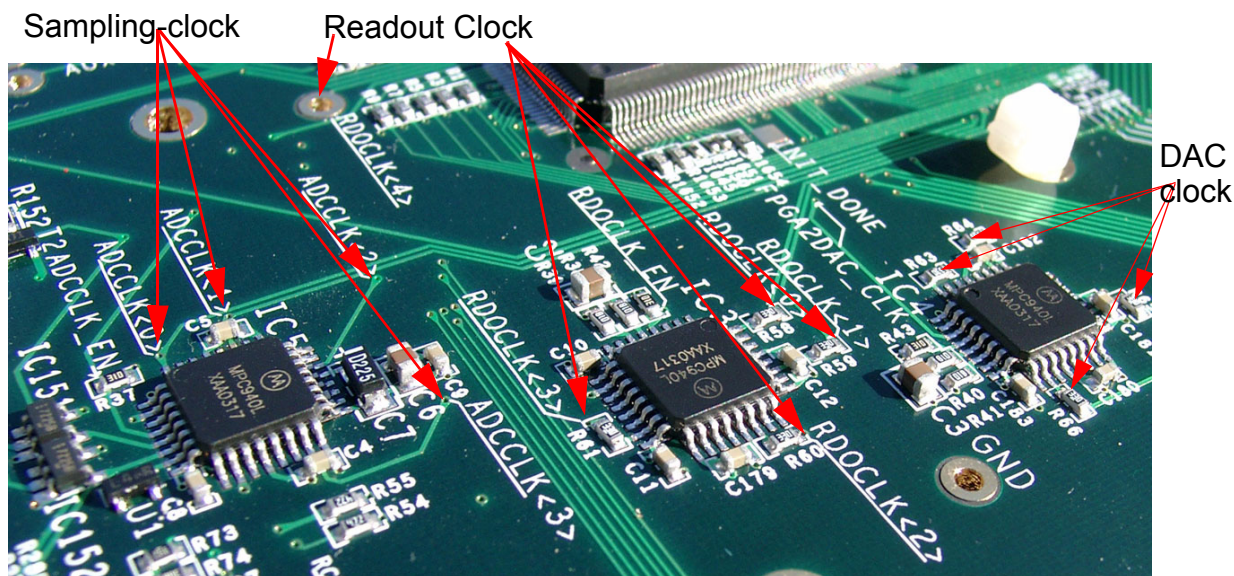


Figure 151 All clock drivers

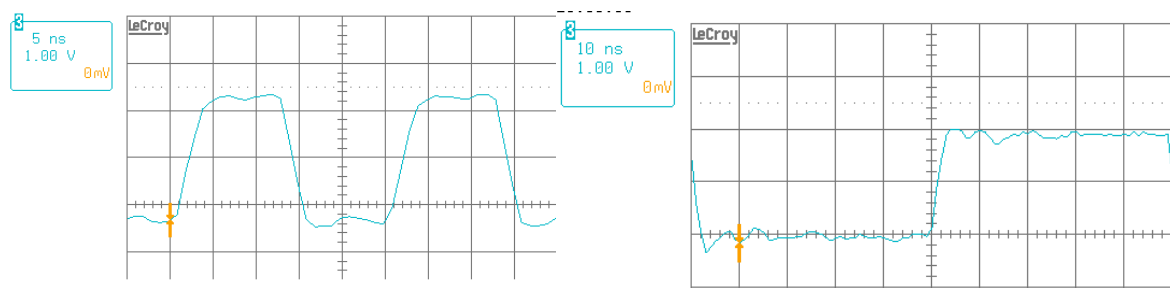


Figure 152 Scope shots of sampling clock (10 MHz) and readout clock (40 MHz)

1. The definition of the sampling clock is matter of the RCU firmware.

18 FEE user control via DCS card

The DCS card is a small Linux sub-system on with standard network, physically implemented as a mezzanine card on the RCU. The DCS card access is opened for a user via

```
ssh root@<DCScardname>.domain
```

The DCS card can be initialized via the DCS_ON command at 0xE000 (Table 15) to become the software master of the RCU. After resetting the FEE, a root user on the DCS card can configure and readout the FEE cards on the hardware programming level. The corresponding RCU-shell is entered via the rcu-sh command.

```
*****
executing: wait 1 s

* Welcome to the DCS Board *
executing: w 0x2002 0x0

*****
executing: wait 1 s

executing /etc/profile
executing: w 0xe000 0x0 #bus control

FIRMWAREVERSION=v2.4uib
executing: wait 1 s

dcs0034:/ $ cd dcs
executing: w 0x2001 0x0

dcs0034:/dcs $ rcu-sh
executing: wait 1 s

open device: using message buffer v2 format for
firmware version 2.4
executing: wait 1 s

current driver version 0.5 - debug
executing: w 0x2001 0x0

executing: wait 1 s

executing: w 0xe000 0x0

*****
enter operation (h/i/q/r/w):

rcu bus easy read/write access
terminating batch processing, please wait ...

version 1.4 (compiled Feb 15 2006, 15:50:09)
enter operation (h/i/q/r/w):

Matthias Richter, University of Bergen

Matthias.Richter@ift.uib.no

enter operation (h/i/q/r/w):b init.scr
```

Figure 153 Screenshot of system reset via the RCU-shell on the DCS card

A screenshot of the standard initialization including execution of the init.scr script is shown in Figure 153. The user input is shown in italics (red). User scripts have the extension .scr and can be executed via the command

```
b <scriptname>.scr
```

The rcu shell is not meant to be multi-user and may hang up if several users access the rcu-sh at the same time. In this case, a new connection to rcu-sh allows to reset the driver via the command

```
rcu-sh driver reset
```

RCU shell scripts on the DCS card may be used to execute a sequence of DCS scripts in a conditional way as shown in the example below for a loop over several DCS scripts:

The embedded DCS scripts “set_hv_0_s4.scr” and “set_hv_0_s4.scr” set all bias voltages to the minimum

```
while true;
do
rcu-sh b set_hv_0_s4.scr;
sleep 2;
#rcu-sh b reset.scr;
#rcu-sh wait 1s;
#rcu-sh b reset.scr;
#sleep 2;
sleep 10;
rcu-sh b set_hv_max_s4.scr;
sleep 2;
rcu-sh b reset.scr;
rcu-sh wait 1s;
rcu-sh b reset.scr
rcu-sh wait 1;
done;
```

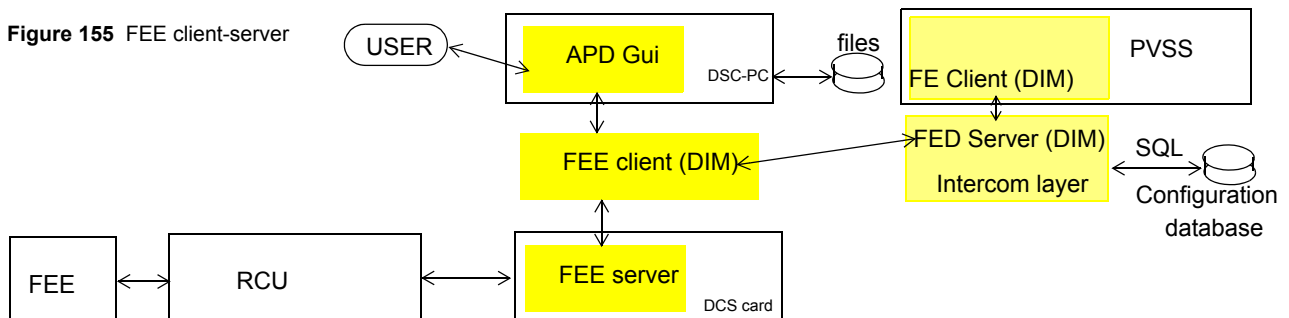
Figure 154 RCU shell script for execution of several DCS scripts

value (210 V) and, after a delay, to the maximum value. This loop test is used as a burn-in for the HV bias circuitry.

18.1 FEE server

The DCS control hierarchy with the FEE server running on the DCS card on the RCU is depicted in Figure 155

Figure 155 FEE client-server



The FEE server can be started locally in the DCS card as follows

```
cd /home/phos
./feeserver start local.sh
```

18.2 Bias Voltage programming

In addition to the standard Altro and RCU register addresses [24], the PCM on the PHOS FEE cards implement a set of 32 new 10 bit read/write registers for setting the bias voltages

Table 9 DAC register correspondence with CSP channel numbers (see chapt 7)

DAC register relative to PCM	CSP channel number	DAC register relative to PCM	CSP channel number
0x40	23	0x50	8
0x41	22	0x51	9
0x42	21	0x52	10
0x43	20	0x53	11
0x44	19	0x54	12
0x45	18	0x55	13
0x46	17	0x56	14
0x47	16	0x57	15
0x48	0	0x58	31
0x49	1	0x59	30
0x4A	2	0x5A	29
0x4B	3	0x5B	28

Table 9 DAC register correspondence with CSP channel numbers (see chapt 7)

DAC register relative to PCM	CSP channel number	DAC register relative to PCM	CSP channel number
0x4C	4	0x5C	27
0x4D	5	0x5D	26
0x4E	6	0x5E	25
0x4F	7	0x5F	24

The DCS script example of Appendix 2. shows how to set Bias Voltages via DAC registers (for Syntax and decoding refer to Paragraph 30) for more details see [15]

The DCS scripts

```
set_hv_max_s4.scr
```

```
set_hv_0_s4.scr
```

set all 32 bias channels of card in address 4 either to the maximum (400V) or to the relative zero voltage (210) Volt.

The example Figure 156 below shows details of a DCS script for setting bias voltages.

The Bias Voltages for each APD are programmed via the 32 PCM register block starting at address 0x40 .

This example sets all bias voltages to 342 Volt and reads back the DAC settings back on Address 3 branch B

```

w 0x7000 0x633040      # send PCM register address 40 ( =CSP 23) to instruction memory
w 0x7001 0x70029A      # send data 29A to register of addr. 40
w 0x7002 0x633041      # send PCM register address 41 ( =CSP 22) to instruction memory
w 0x7003 0x70029A
    e.t.c .....
w 0x703E 0x63305F      # send PCM register address 5F ( =CSP 24) to instruction memory
w 0x703F 0x70029A
wait 1 us
w 0x7040 0x63301E      # write 0x0000 to address 1E as command to update high voltages
w 0x7041 0x700000      # second part of above 40 bit Altro write instruction
wait 1 us
w 0x0 0x0              # execute / update the registers
r 0x7800               # check error and status register ( must be 0 )
w 0x6C01 0x00          # clear the error status register
////////////////////////
# read back the DAC registers .....
w 0x7000 0x533041      # send instruction to read PCM register at address 40 to instruction memory
w 0x7001 0x533042      # send instruction to read PCM register at address 41 to instruction memory
# ..... etc.. send all read instructions of registers 42..5F to instruction memory
w 0x701F 0x53305F      # send instruction to read PCM register at address 5F to instruction memory
w 0x7020 0x390000      # end of script
wait 1 us
w 0x0 0x0              # execute script list from offset 0x0
wait 1 us
r 0x7800               # test Altro ERRST (error status register) must be 0
r 0x6000 32            # display 32 times data read from the registers
# ..... get 32 DAC register listed
w 0x6C01 0x00          # reset ERRST register

```

Figure 156 Example of a DCS script for setting Bias Voltages

19 Firmware programming of PHOS devices

A PHOS readout system consists of FEE and TRU cards and of RCU cards with SIU and DCS mezzanines (outside of the PHOS module). Each of these devices (FEE, TRU, SIU, DCS and RCU) are to be programmed with firmware or firmware updates.

The programming of FEE cards (PCM in Altera FPGA) requires either USB programming functionality or an Altera Byteblaster II cable, connected to the Jtag connector (see 19.1 .) Once the Flash (EPC16) of the FEE is programmed, it is permanent such that a power-on cycle of the FEE cards automatically reloads the programmed firmware version. The firmware files have the expansion .pof for the Flash and .sof for the FPGA.

Note: the FEE serial number resides in the plug-in USB Prom 24LC256 (IC 146) .

The programming of the RCU-4 Xilinx chip requires a Xilinx parallel cable IV for Boundary Scan mode programming via the Xilinx Impact software(see 19.3 .) The firmware files have the extension “.bin”. The programming of the TRU (Trigger Algorithm in Xilinx FPGA) requires either USB functionality or a Xilinx parallel cable IV for Boundary Scan mode programming via the Xilinx Impact software. The firmware has the extension “.bin”

The programming of the DCS card (see 19.2) requires an Altera Byteblaster II adapter and the exc_flash_programmer program as part of the Altera Quartus Installation for windows. The firmware has the extension “.hex”.

19.1 Firmware programming of the PCM board controller

The FEE board must have digital 3.3Volt enabled, this is normally enabled by presence of the GTL bus with RCU mastership. For verification that 3.3Volt and 2.5 Volt are availability on the FEE board, the signal MPS_enable (Figure 108) must be high, thereafter the Flash and PCM can be programmed via the JTAG connector.

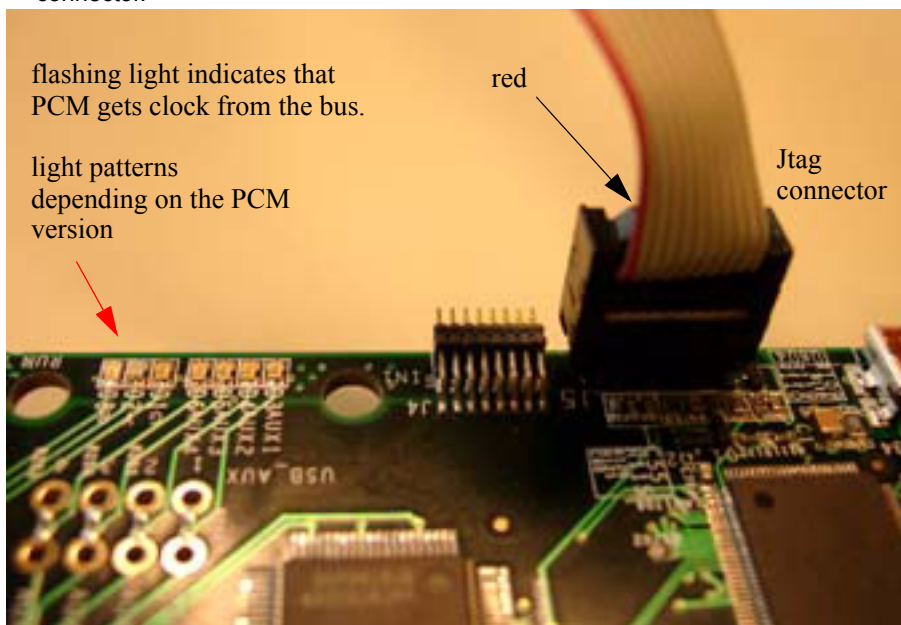


Figure 157 LED indicators and JTAG connector

The Quartus Programmer software via parallel port cable (which must interfaced via a Byte blaster II adapter cable) is required to program the *RCU.sof* and *RCU.pof* files for the EPC16 K Flash and EPK FPGA (this order is important).

After successful PCM programming, the availability of the RCU (or USB) clock results in a flashing LED if the clocks are provided. After reset, the FEE card reloads the programmed PCM version from it's Flash. The

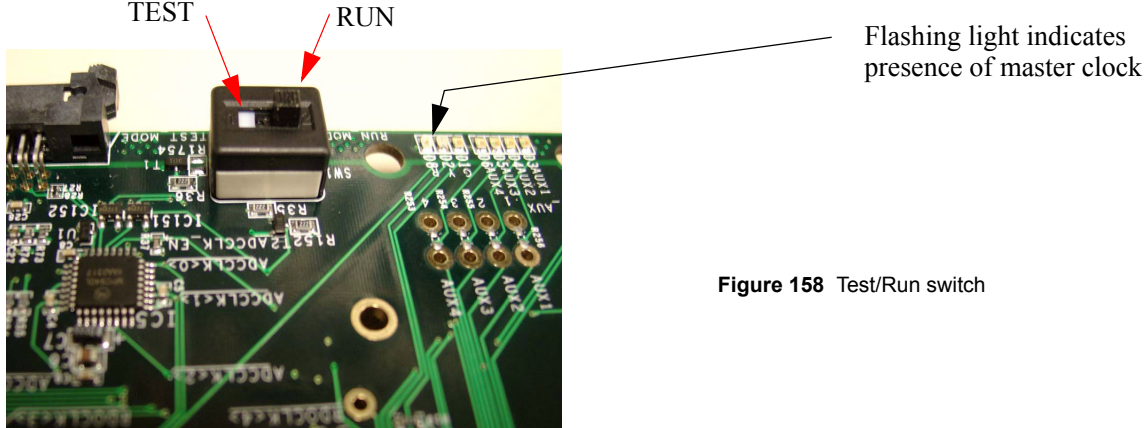


Figure 158 Test/Run switch

RUN/Test switch must be in position RUN for RCU -based test situations, and in TEST mode for USB based test situations

The hardware setup screen for preparing to programming is shown in Figure 159 .

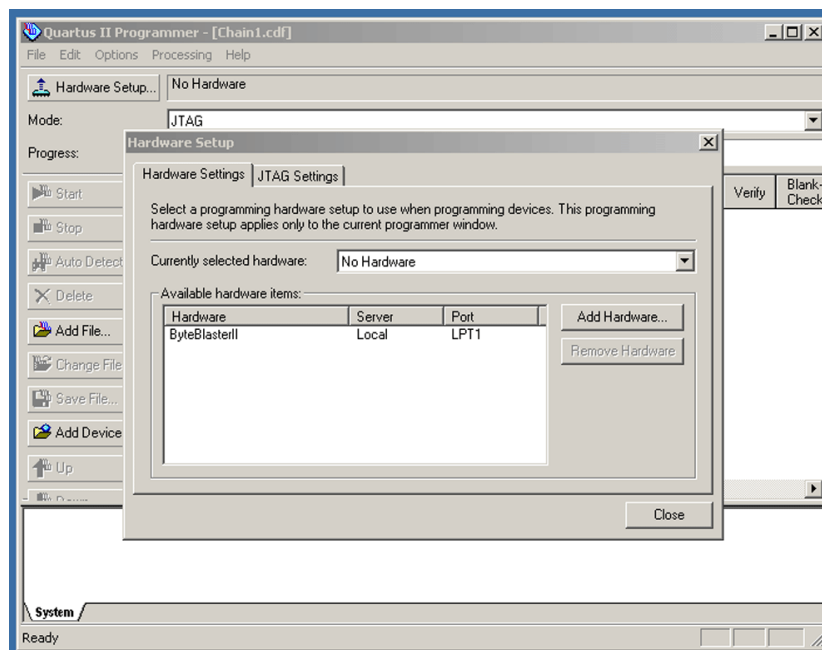


Figure 159 Quartus Byteblaster Configuration

The “.po” and “.sof” configuration files are added via the *add file* button and the associated file browser. The top-down order of the programming must be 1.) Flash (EPC16) 2.) FPGA (EP1K..)

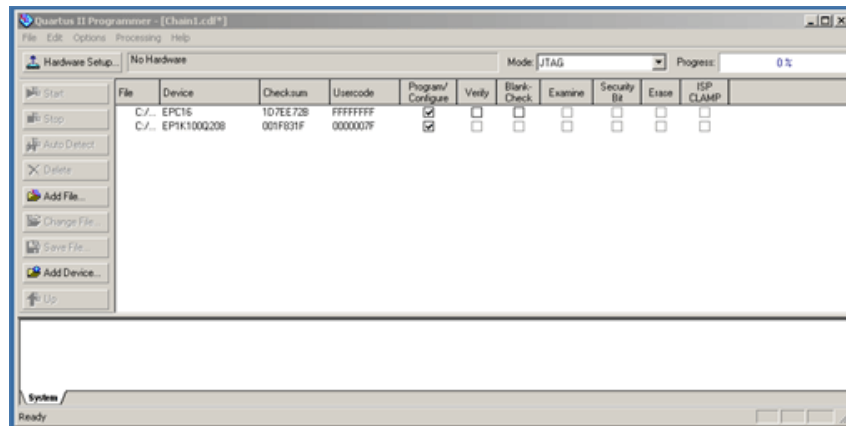


Figure 160 Quartus Byteblaster “Add file” screen for FEE cards

Click the “start” button to start programming and observe the messages in the system screen.

19.2 Firmware programming of the DCS Linux card [2]

The hardware connections for the DCS card 1.52 is shown in Figure 161. Note that PHOS and EMcal require **for Byteblaster connection**

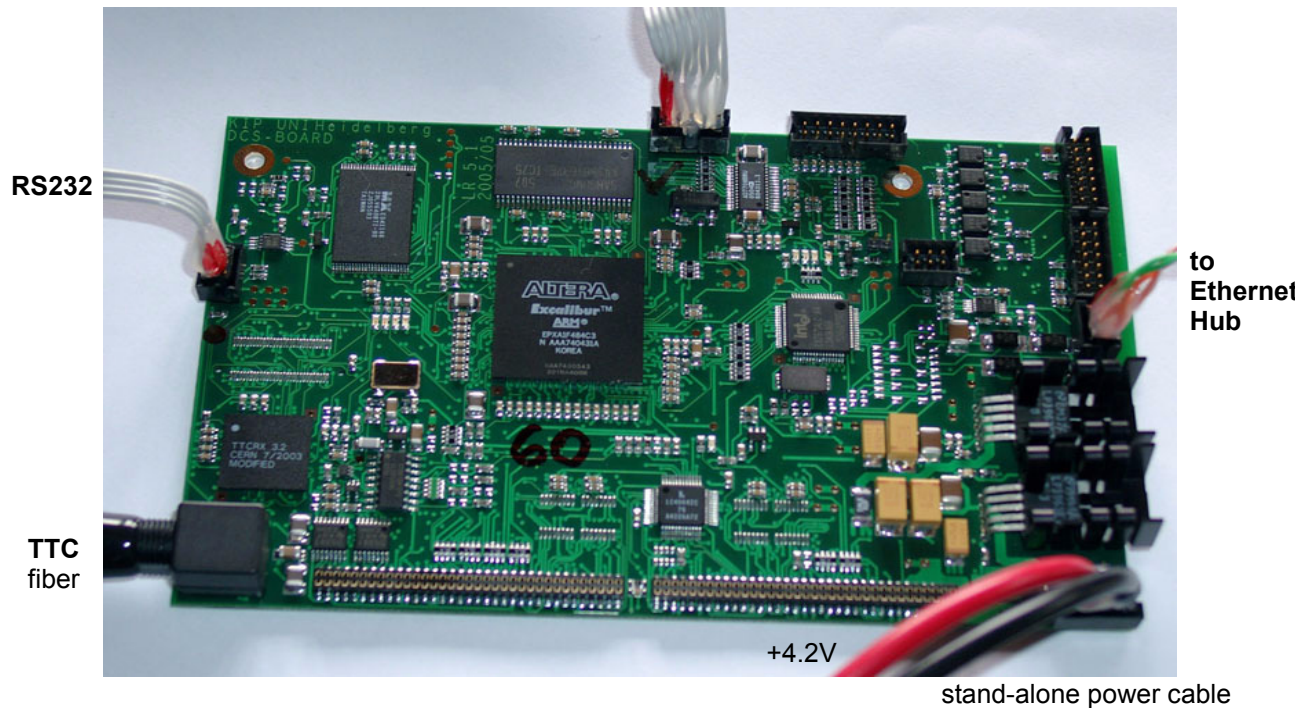


Figure 161 Photo of DCS card (TPC version 1.52)

DCS cards which are configured for the TPC (not TRD!)

The Flash must be programmed with EPXA1 Linux configuration file of the Altera Excalibur FPGA, which must also contain the specific MAC address of the card. This MAC address is coupled to the serial number of the DCS card [2]. For getting this specific file it is possible to get card-specific hex files from <http://frodo.nt.fh-koeln.de/~tkrawuts/dcs.html>. Completely configured hex files (with uib extension) for PHOS are provided by the University of Bergen <http://www.ift.uib.no/~alme/> (see also [12])

For programming the DCS Flash with the configuration file ".hex", use the Altera Quartus exc_flash_programmer.exe file on Windows systems (in the /bin directory of Quartus installation), connect the DCS card via an Altera Byteblaster II adapter and run the programming command as DOS shell command:

```
exc_flash_programmer -p -v -g file.hex
```

It is also possible to read back a hex file from the flash (for backup)

```
exc_flash_programmer -r 0x400000 readbackfile.hex
```

For clearing the Flash use:

```
exc_flash_programmer -a
```

19.3 Firmware Programming of RCU

The RCU must be programmed via a configuration file residing in the DCS card. For tests of firmware versions,

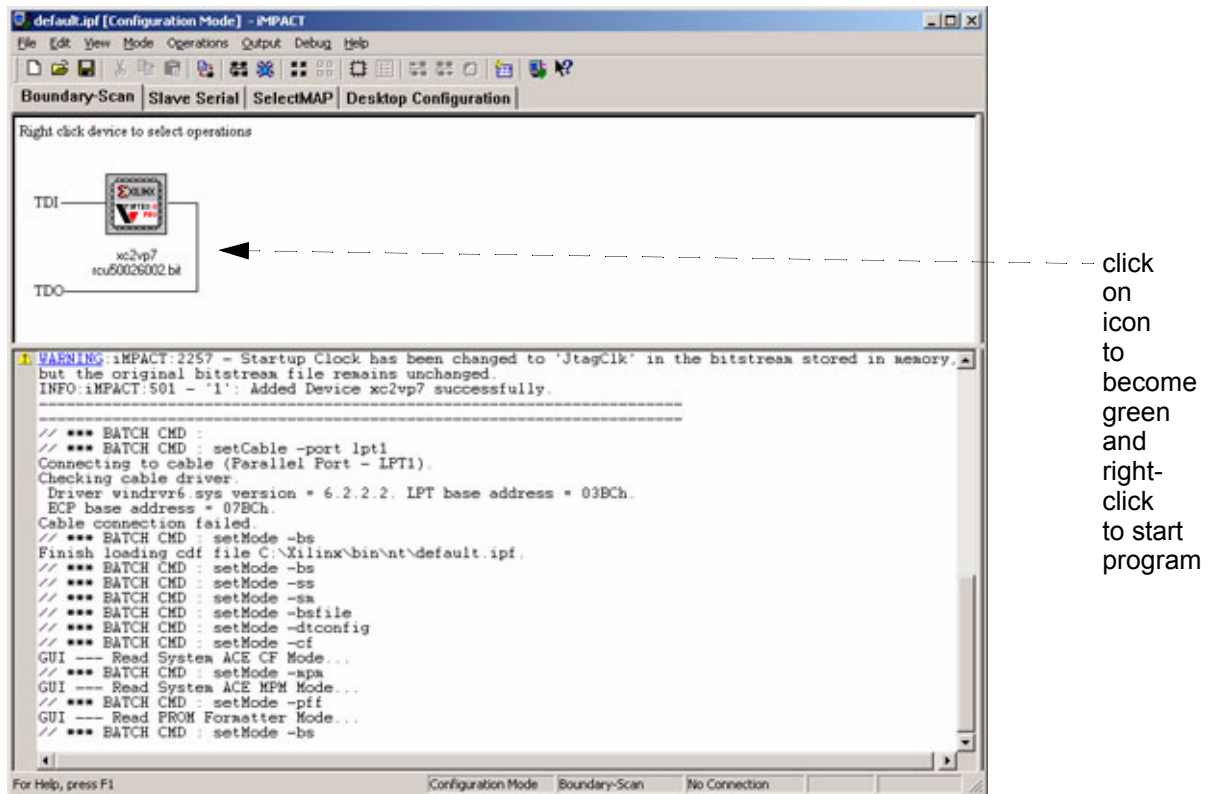


Figure 162 Xilinx Impact configuration screen for RCU with bitfile rcu50026002.bit

the Xilinx FPGA on the RCU's can be loaded using the Xilinx Impact software (see Figure 162) and a Xilinx programmer cable. **However after a power cycle, the version stored in the Actel Flash will be reloaded!**

For programming the Actel Flash see chapter 19.3.1

The configuration file is of type “.bit”. A Xilinx Parallel Cable IV (reference XLXHW-PC4) with connector for a parallel port of a computer and a +5V power adapter (keyboard connector or USB) is needed. The flat cable of the device mates mit the JTAG connector on the RCU. The LED on the device must become green, (check 5 Volt power is provided by the FEE) before programming can be successful.



Figure 163
Xilinx parallel cable IV

Figure 162 depicts the screen of the Xilinx Impact tool in Boundary Scan Configuration mode, after the parallel cable IV has been successfully initialized and connected and the Jtag chain was initialized, detecting the Xilinx device xc2vp7 (the FPGA on the RCU). In order to program, right click on the device (becomes green) and select program¹. The programming finishes by giving the message “Programming successful”.

19.3.1 RCU bit files

The latest RCU files are available under

<http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc/firmware.htm>

The latest version (July 2007) that allows using NIM triggers via the NIM mezzanine card is 181206

The version actually loaded in the FPGA can be read from register 0x8008

TPC and PHOS use the same firmware, however PHOS has a different FEE card addressing scheme than TPC. This is taken care by the register 0x8009 which is to be loaded with 0x1 for PHOS mode.

Note: if one cannot initialize the FEE card in the first or last GTL bus slot this is most likely due to the RCU firmware being in TPC mode. Change it by writing 0x1 into register 0x8009

1. Note: the “verify” button should be disabled.

19.3.2 Programming the RCU flash via the DCS card

For reprogramming the Actel flash on the RCU, one needs the RCU bitfile and a corresponding configuration file in the DCS card. Then on the DCS card apply the following steps

Go to folder RCU_FW (may also have a different name)

- Remove the bit file already there (it consumes a lot of space)
- Copy the new bitfile to this directory
- Edit the flashconf file to match the new filename
- execute rcu-sh b prepare_rcu
- execute: ./rcuflashprog flashconf
- execute: rcu-sh w 0xb000 0x4 (programming the board)
- execute: rcu-sh r 0x8008 (reading the version number)

This should now read the new version of the RCU firmware which is also retained after a power cycle

In case the configuration file is corrupted or absent, the following procedure has to be applied:

Download the package: <http://www.ift.uib.no/~alme/wiki/rcuflashprog.tar>

Store the following files in the /rcu/ folder on the DCS boards:

rcuflashprog - an executable file
flashconf.txt - the configuration file for the tool

Copy the RCU bit file to be used for configuration to the dcs board /rcu folder

Edit flashconf.txt so that the file name and path for the bit file is correct. (use vi on the dcs board, and ONLY change path_icfile and name_icfile variables)

```
#init program file
enable_icfile = true
path_icfile = /rcu/
name_icfile = rcu_190606.bit
startaddr_icfile = 0h
```

Clear the Xilinx FPGA with the following command:

```
rcu-sh w 0xb002 0x1
```


Execute the rcuflashprog:

```
./rcuflashprog flashconf.txt
```

First it will erase the flash, then write the new file to the flash. When you have control over the commandline again, it is finished. To upload the new firmware from the Flash Memory to the Xilinx simply type:

```
rcu-sh w 0xb000 0x4
```

20 Shaper implementation options [6]

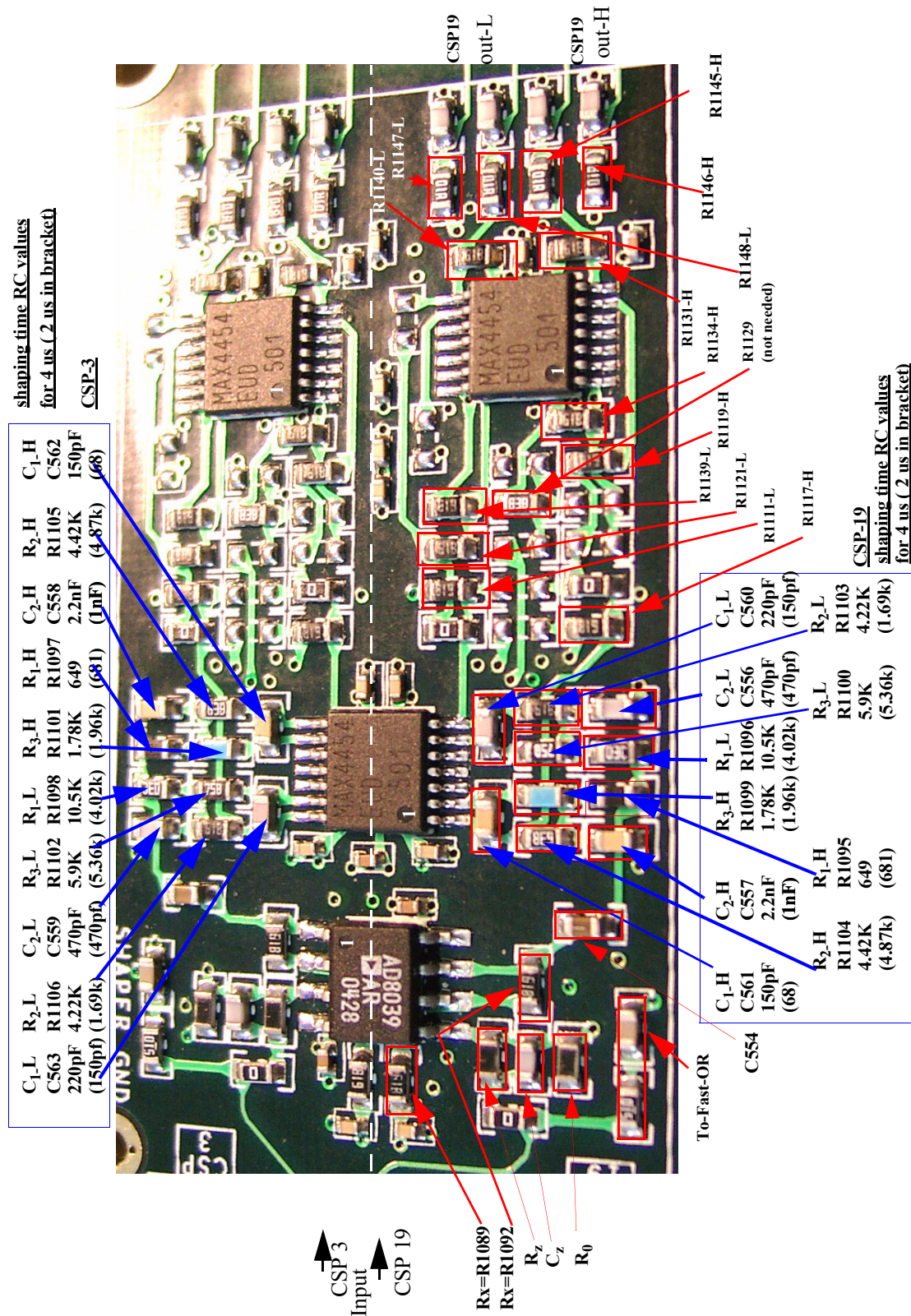


Figure 164 CW shaper component placement for 4us and (2us). The R/C names correspond to the serigrafie on the PCB.

The shaping time and gain options on the CW shaper can be calculated as described in [2][6]

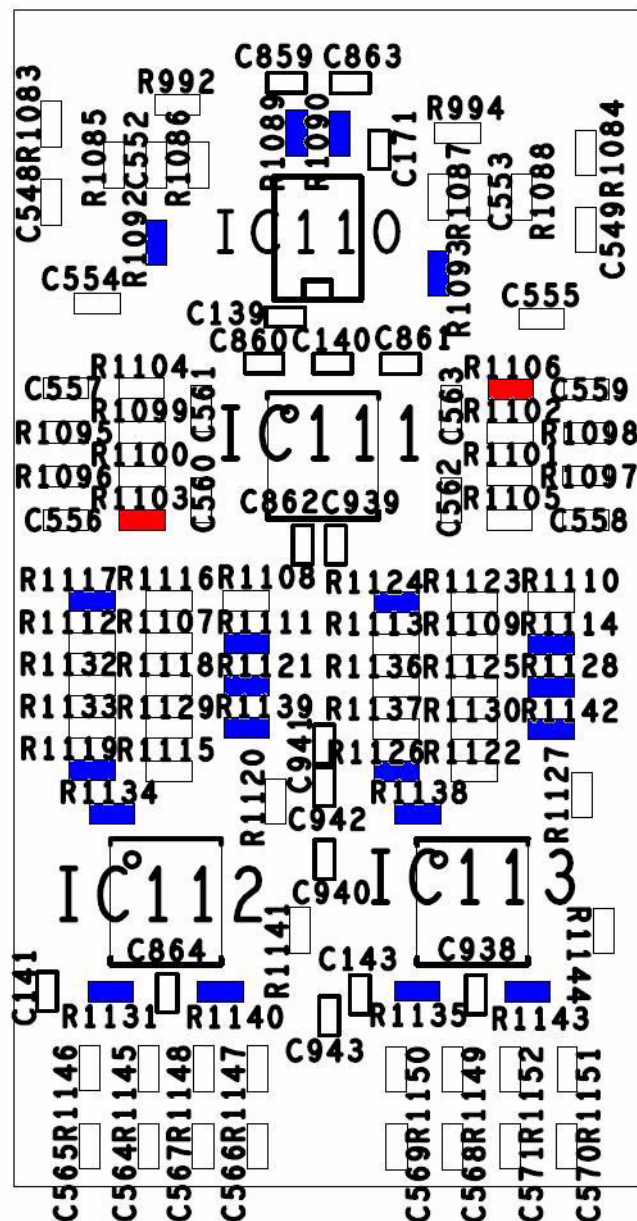


Figure 165

Serigrafie on FEE V1.1a for R and C components on one dual shaper macro. This corresponds to the CSP 3 and 19 and is a template for all other shapers macros

Depending on APD and CSP temperature, the minimum of the noise is a function of the shaper time constant. The components for the 2 μ s and 4 μ s options for the PHOS shaper are detailed in Figure 164 together with the 0.2 μ s shaper of EMCal. The Serigrafie printed on the FEE card V1.1 for the shaper macro CSP3/19 is shown in Figure 165

20.1 Schematics of a single shaper channel

Each of the 32 CSP input signals is amplified and split into 2 separately implemented CW shapers[6] of high and low gain with a nominal gain ratio 1/16 (for measured gain ratio see [25]). The input stage is a pre-emphasis network (R_z, C_z, R_o) followed by a gain buffer. The 2nd order -integrator with Bessel transfer characteristic is implemented as multi-feedback configuration with a single MAX 4454 operational amplifier. A differential driver with following anti-alias filter interfaces to the Altro 10 bit ADC which

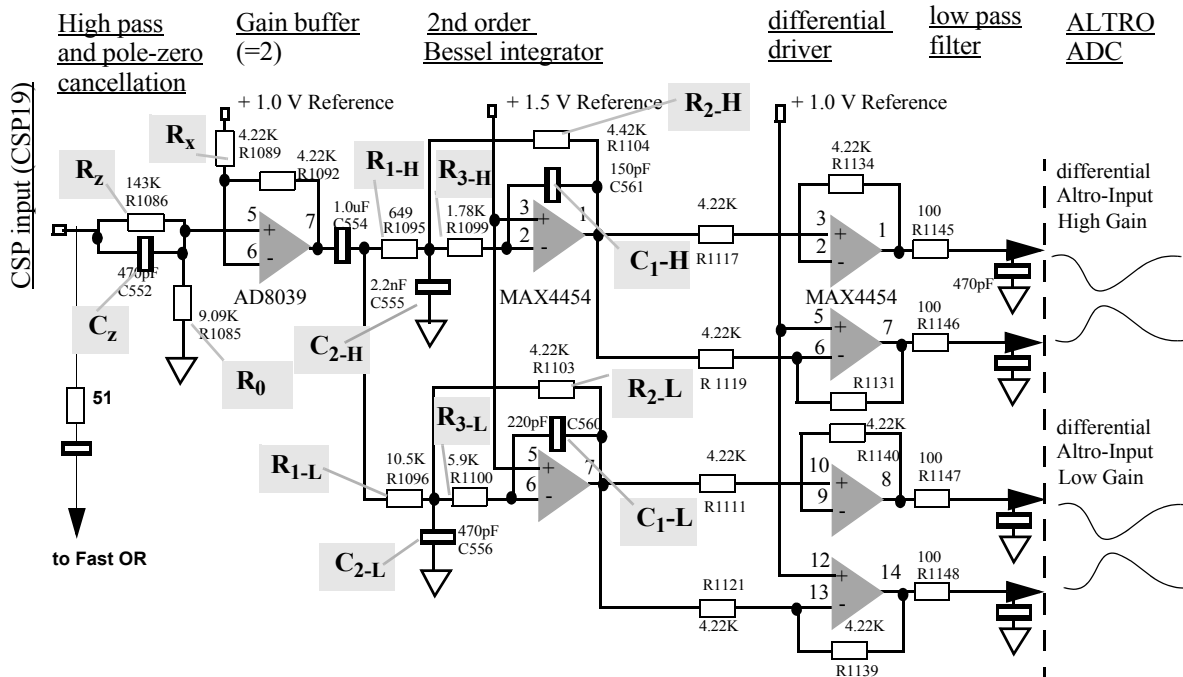


Figure 166 CW Shaper schematics for CSP 19 channel on FEE V1.1

measures the complementary shaper outputs of 1 Volt swing each (2 Volt total) against a reference voltage of nominally 1.035 Volt (see chapter 17) plus some pedestal offset. Pedestals in the order of 30..40 ADC counts are needed in order to measure undershoot and noise without cutoff.

The specific R-C values for the CW shaper options are shown in Table 10 below.

Table 10 RC values for CW shaper 4 us, 2 us and 0.2us peaking time (buffer gain = 2, gain ratio =16) For calculation of different peaking times refer to Alice Note on FEE electronics

CW Phos	Shaper <i>4us</i> shaping time =2us								
bom Reference	R1095	R1104	R1099	C561	C557	C552	R1086	R1085	R1089/1092
R/C Name	R1-H	R2-H	R3-H	C1-H	C2-H	Cz	Rz	R0	Rx
HG= 2*3.35, $\tau_{peak} = 4.1$ us	649	4.42 k	1.78 k	150pF	2.2 nF	470pF	143 k	9.1 k	4.22K
	R1096	R1103	R1100	C560	C556				
Low gain	R1-L	R2-L	R3-L	C1-L	C2-L	-	-	-	-
Low gain 2*0.21 $\tau_{peak} = 4.06$ us	10.5 K	4.22 K	5.9 K	220 pF	470pF	-	-	-	-
CW Phos	Shaper <i>2us</i> shaping time $\tau=1$us								
bom Reference	R1095	R1104	R1099	C561	C557	C552	R1086	R1085	R1089/1092
R/C Name	R1-H	R2-H	R3-H	C1-H	C2-H	Cz	Rz	R0	Rx
HG=2* 3.35. τ_{peak} =2.04 us	681	4.87 k	1.96 k	68 pF	1n F	470pF	143 K	4.22K	
bom Reference	R1096	R1103	R1100	C560	C556				
Low gain	R1-L	R2-L	R3-L	C1-L	C2-L	-	-	-	-
LG= 2*0.21 τ_{peak} =2.04 us	4.02 K	1.69 K	5.36 K	150 pF	470 pF	470pF	143 K	4.22 K	
CW Emcal	Shaper <i>0.2us</i> shaping time 100 ns								
Bom Reference	R1095	R1104	R1099	C561	C557	C552	R1086	R1085	R1089/1092
R/C Name	R1-H	R2-H	R3-H	C1-H	C2-H	Cz	Rz	R0	Rx
High gain 2* 3.35 $\tau_{peak} = 2.04$ us	75	309	196	100 pF	1n F	470 pF	143 K	422	
bom Reference	R1096	R1103	R1100	C560	C556				
Low gain	R1-L	R2-L	R3-L	C1-L	C2-L	-	-	-	-
Low gain 2*0.21 $\tau_{peak} = 2.04$ us	732	180	330	220 pF	470 pF	470 pF	143 K	422	

The measured shaper outputs for the 3 peaking times and under different test conditions are shown in Figure 167

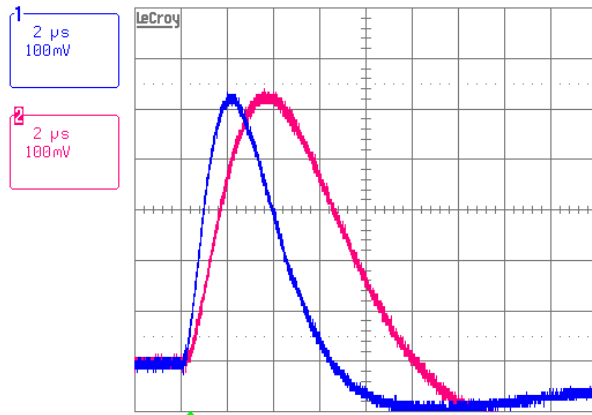
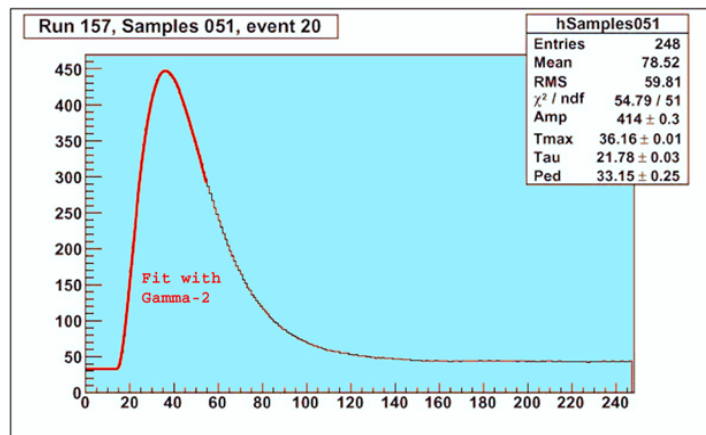
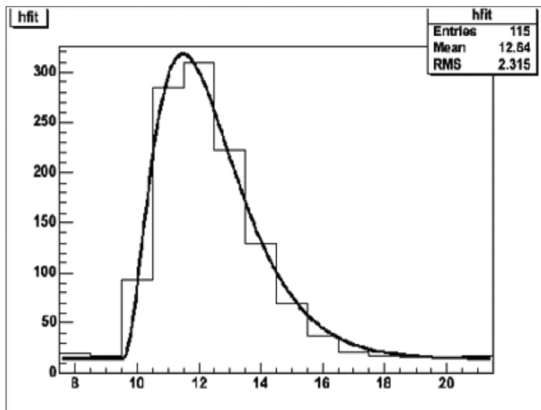


Figure 167 Shaper pulse shapes obtained for the 3 peaking times 4us, 2 us, 0.2 us. LEFT: measured at the input of the ALTRO ADC: 2us and 4 us shaper pulses. Note the undershoot due to artificial step pulser input.

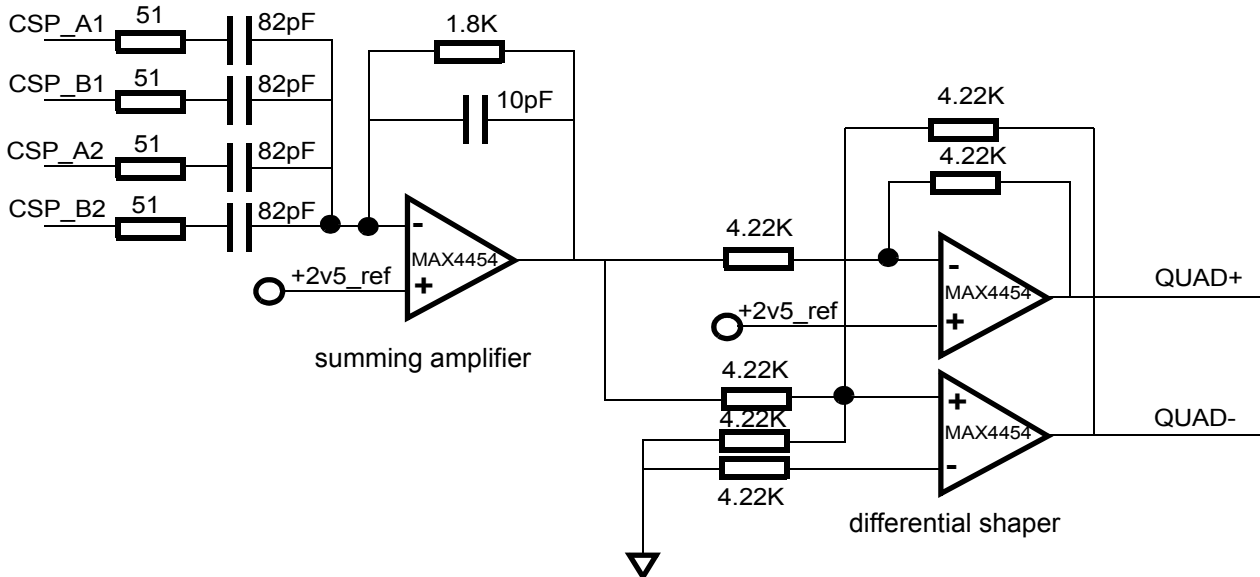
BOTTOM LEFT: offline fit to EMCal shaper with LED and 200 ns peaking time.

BOTTOM RIGHT: Offline fit of PHOS 2us shaper signal with LED.



21 Fast OR

The “Fast Or” is a simple quad shaper which strips off four CSP signals from the shaper input (see Figure 166)



and sums these 2x2 CSP signals into a single Fast -OR signal of 100 ns width. With 32 CSP input channels there are 8 Fast Or output channels, made available as differential signals on a 16 pin connector (J4). The fast or signals transmitted via flat cables of equal length (40 cm) to the TRU trigger Unit.

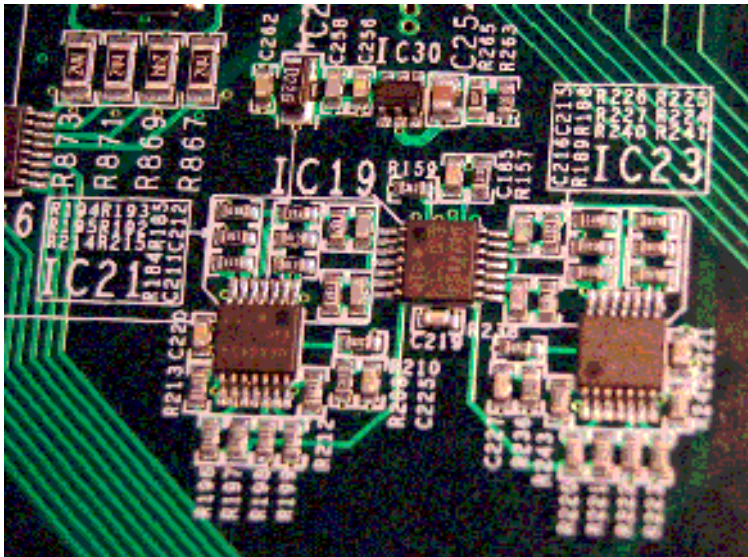


Figure 168 Fast OR group on the FEE card

The FAST OR pulse saturates at ca. 2.3 Volt. The Fast Or gain is 1.33.

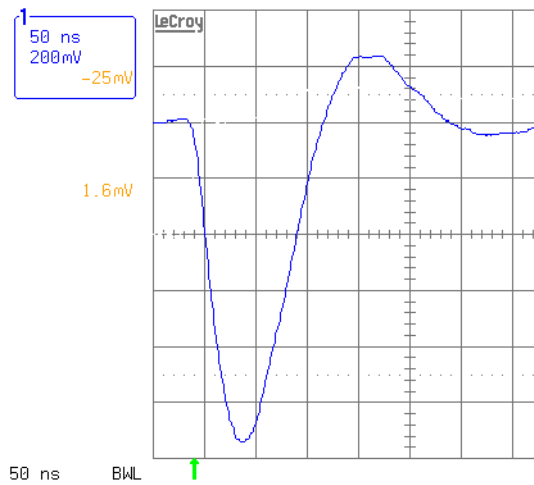


Figure 169 CSP voltage step (pulsar generated) and corresponding Fast OR shaper output.

Figure 169 shows a typical fast-or signal shape which has an amplitude which is proportional to the charge in 2x2 crystals. The over-shoot is due to the CSP overshoot signal.

21.1 Fast OR dynamic range PHOS

For PHOS, the CSP step function voltage depending on light intensity input is according chapter 1.10.1 :

$$U \text{ (CSP)} = 26.7 \text{ uV/MeV}$$

With the gain of the fast-OR shaper (1.33) and the voltage divider gain in front of the ADC on the TRU (0.734) the entrance of the ADC sees 26.3 uV/MeV

The fully differential ADC range is 1V, which means 0.5V for the positive Fast Or input.

The maximum light intensity corresponding to 0.5V is then $0.5/29.3=19 \text{ GeV}$.

Due to shower leakage, the effective maximum energy is higher.

22 T-card connectivity

The purpose of the T-cards is to group the signals to and from a group of 8 or 16 CSP's and to connect all of them via a single flat cable to the FEE front connectors J2 and J3. At the same time the T-card carries RC filters for the HV bias and for the power supplies.

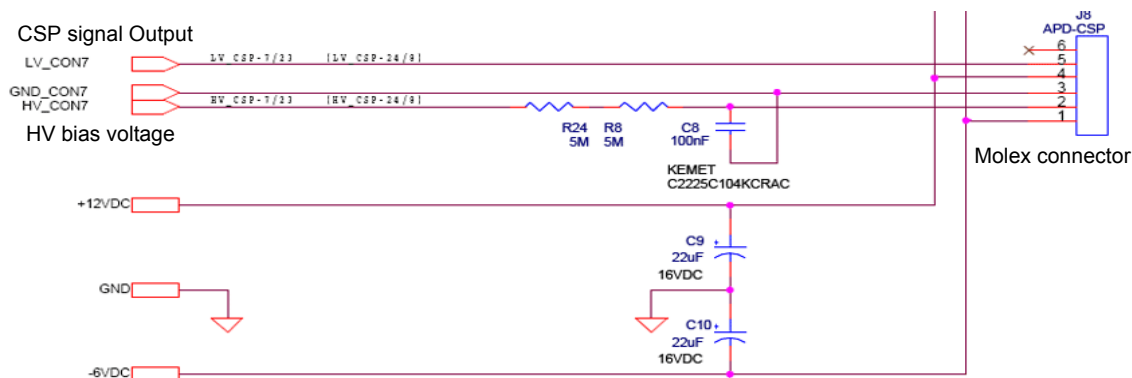
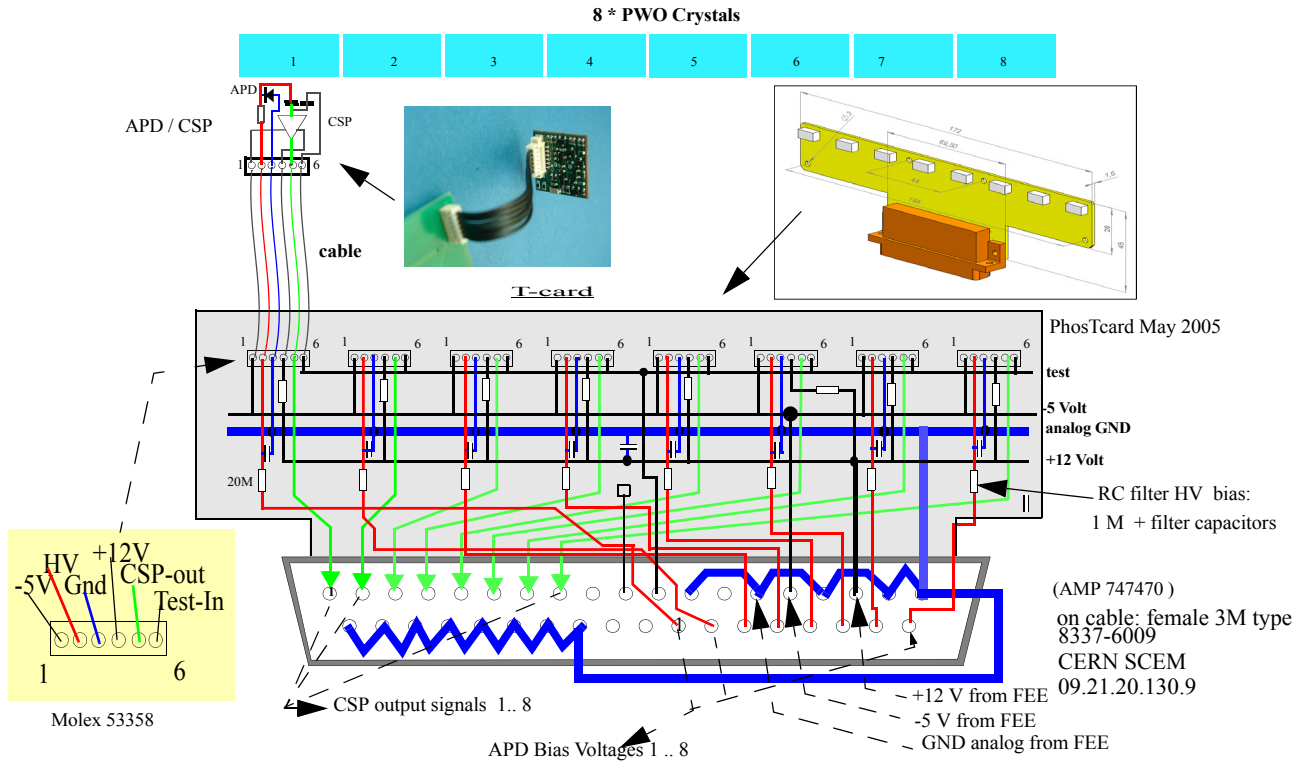


Figure 170 schematics of one CSP channel on a T-card

The PHOS charge sensitive peamplifiers CSP are one unity with the APD diode on their backside. They are connected via a 6 pin jumper cable to the T-Cards. The pinout of the jumper cable is shown in Figure 170 and Figure 32.

22.1 Old 8 channel T-card

The PHOS T-cards are connected via 6-wire jumper cables to a row of 8 CSP's as shown in Figure 171. One



T-card connects 8 CSP preamplifiers to a common 37 wire flat cable which is on its far end connected to the IPCB.

22.2 New 16 channel T-card

The new double T-card have 8 Molex connectors on one side and 8 on the other side. A 60 wire IDC cable

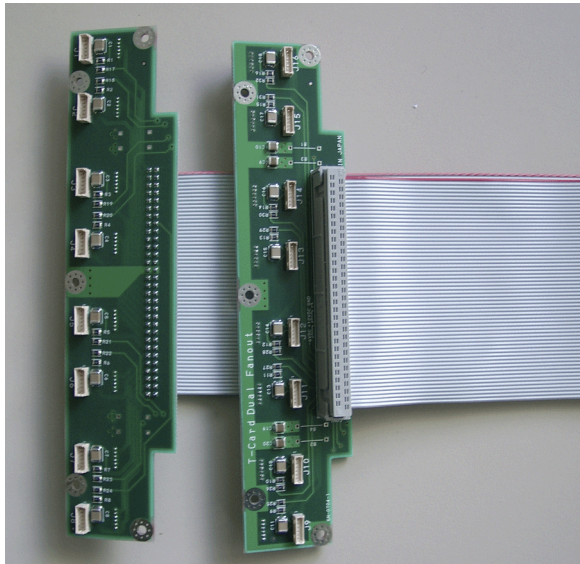
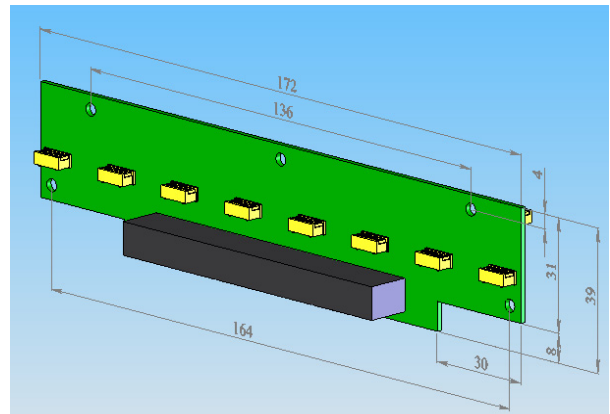


Figure 172 Photo of double T-card both sides



connects the T card to the FEE adapter.

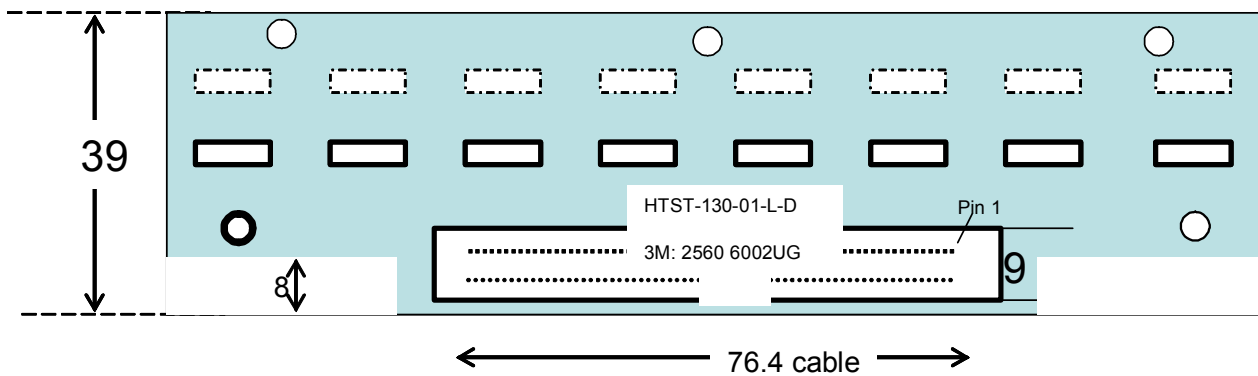


Figure 173 Outlines of new T-card

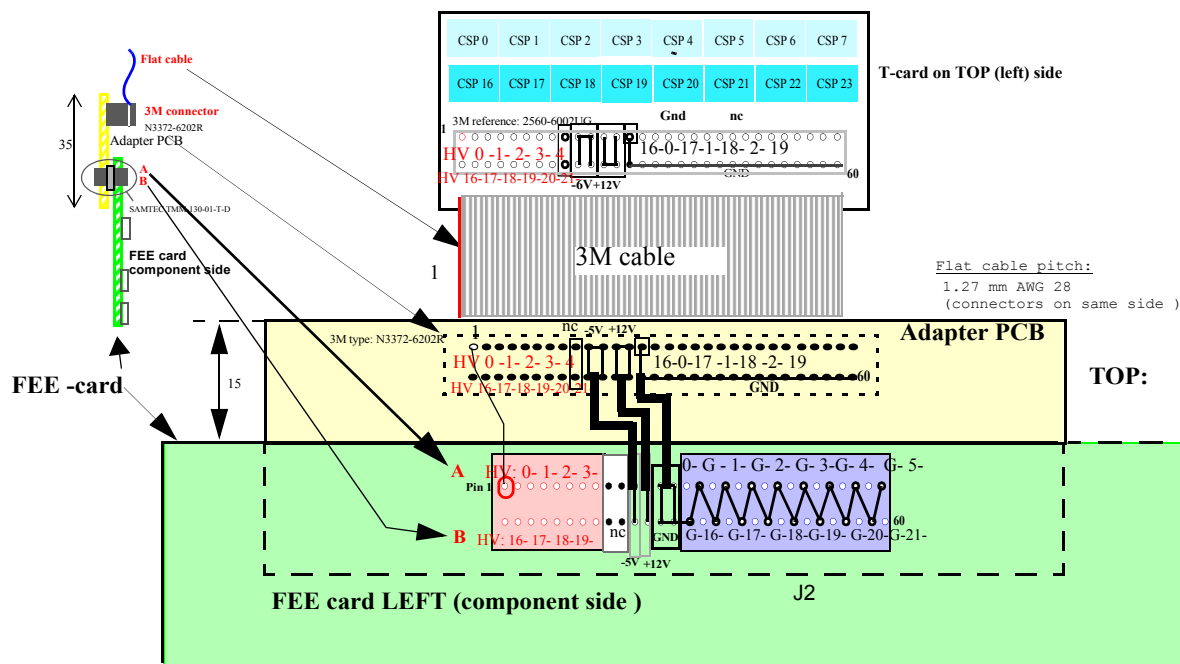


Figure 174 New double T-card connection to the TOP adapter (J2) of the FEE card.

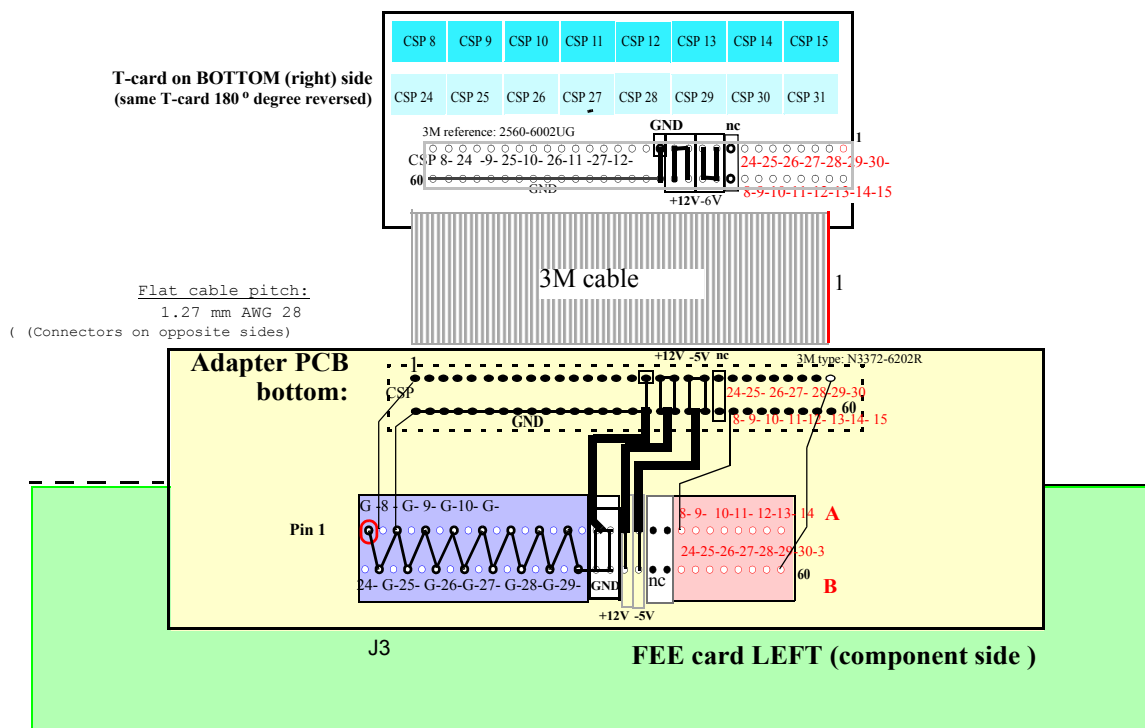


Figure 175 New double T-card connection to the TOP adapter (J3) of the FEE card.

23 Intermediate PCB (obsolete on new PHOS modules)

The detailed pinout of the two FEE card front signal connectors is shown in Figure 176. The connectors are

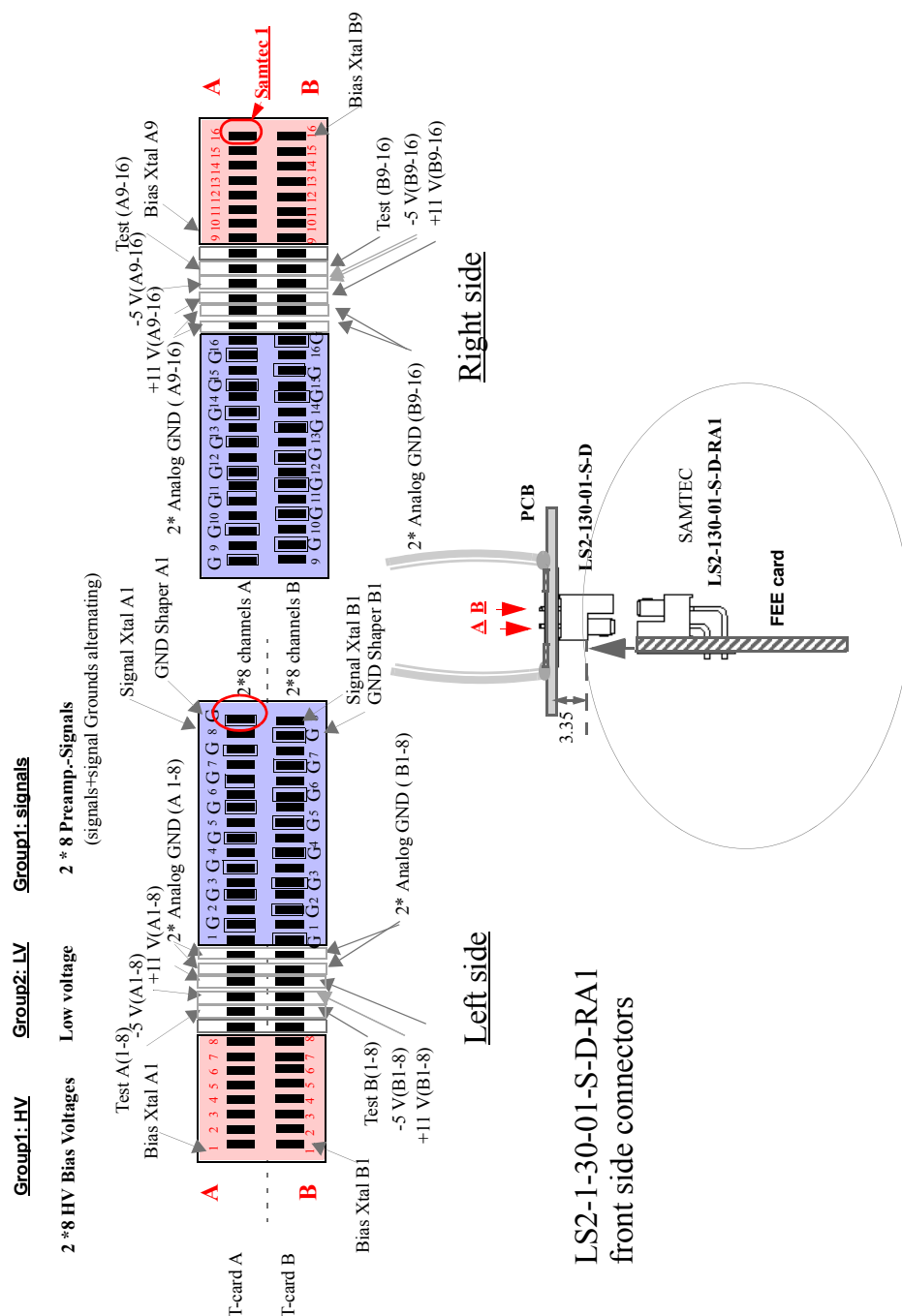


Figure 176 Signal groups in feedthrough connector (Left side view from FEE card to T-card)

“left-right” rotated with respect to their pinout such that High Voltage lines do not cross signal lines. As a consequence, T-cards are 180 degrees rotated for the left and right side connector of the FEE cards. The two parallel rows of FEE connector pins are A and B.

The detailed signal routing between the FEE cards and the crystals, numbered according to the CSP numbering

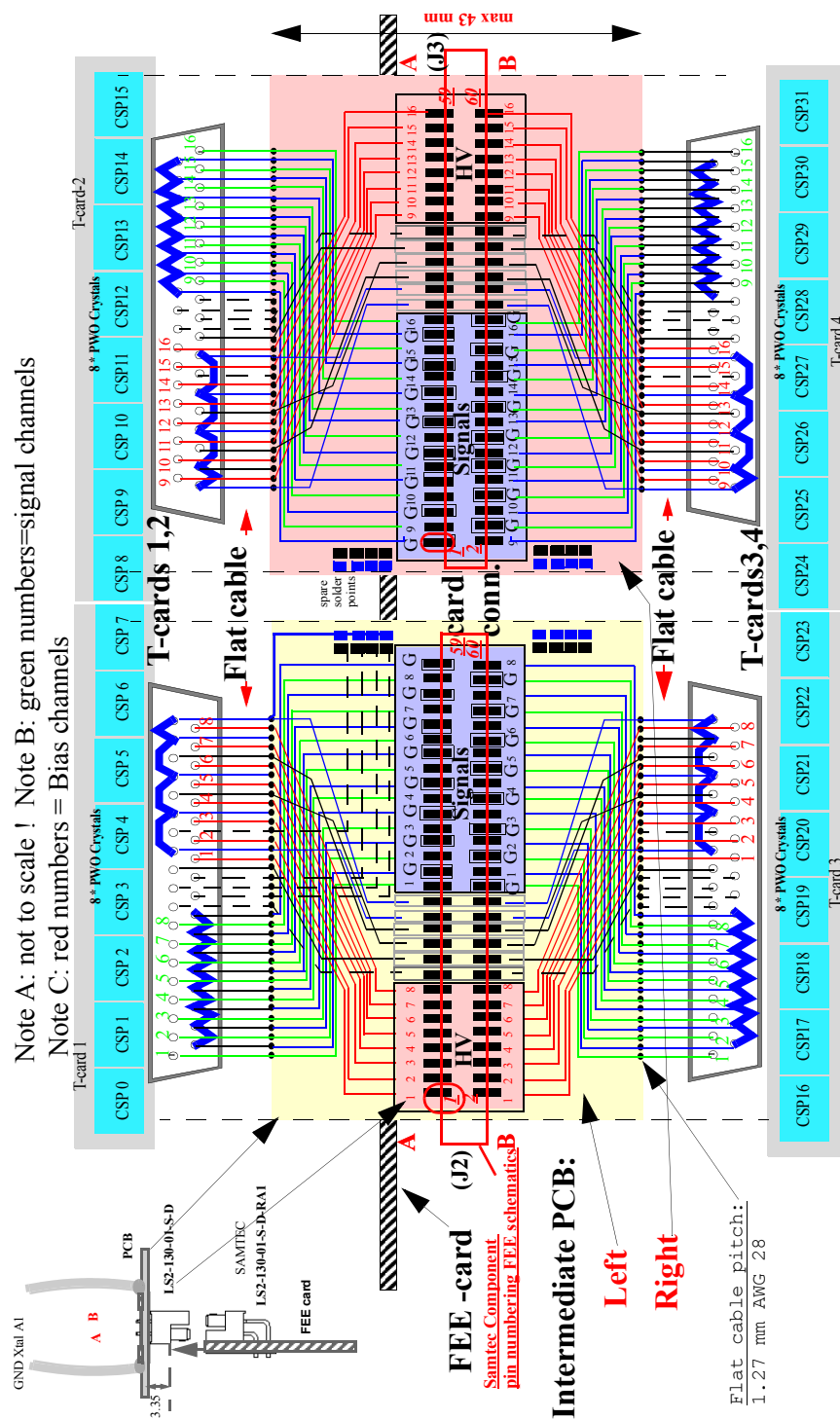


Figure 177 Signal routing between CSP and FEE card via Intermediate PCB

convention and T-card numbering of Figure 182 is detailed in Figure 177

The connector scheme between T-cards and FEE card via the IPCB is detailed in Figure 178

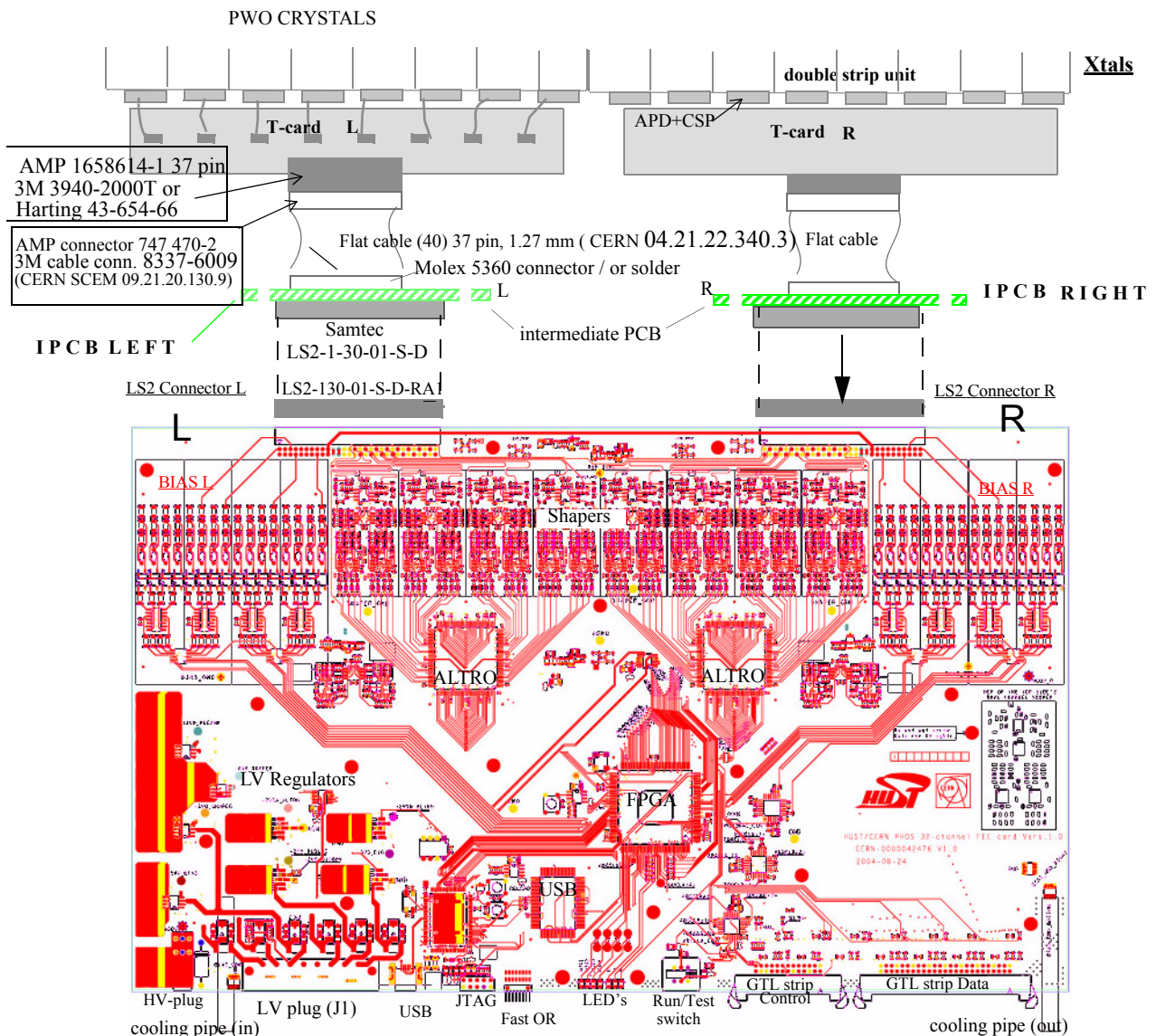


Figure 178 Layout of FEE card and Crystal mapping with FEE shapers

The mapping of FEE card pinout to the PHOS T-card pinout is implemented via hardwired Intermediate PBC's cards (IPCB) which carry the Samtec LS2-130-01-S-D connectors which mate with the FEE connectors. (Figure 178)

Each connector row A and B of the Samtec connector corresponds to one 40 wire flat cable (1.27 mm IDC cable) which is crimped or soldered.

The IPCB cards inside the PHOS module are produced as long strips which consist of repeated individual IPCB's macros.



Figure 179 Photo of Intermediate PCBs connected to the left and right connectors of an FEE card

Figure 181 and Figure 180 shows details of the IPCB strips which map the external detector channels to the FEE card pinout. The FEE card connectors are called “left-side” and “right-side” connectors as defined in Figure 70. The connectors are soldered on the opposite side not shown here, both in the same orientation with pins on side B and holes on side A !.

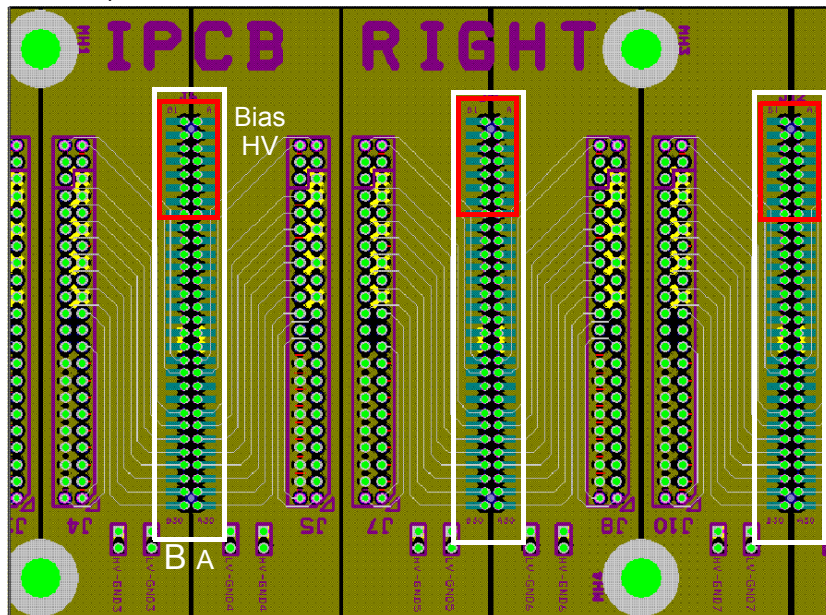
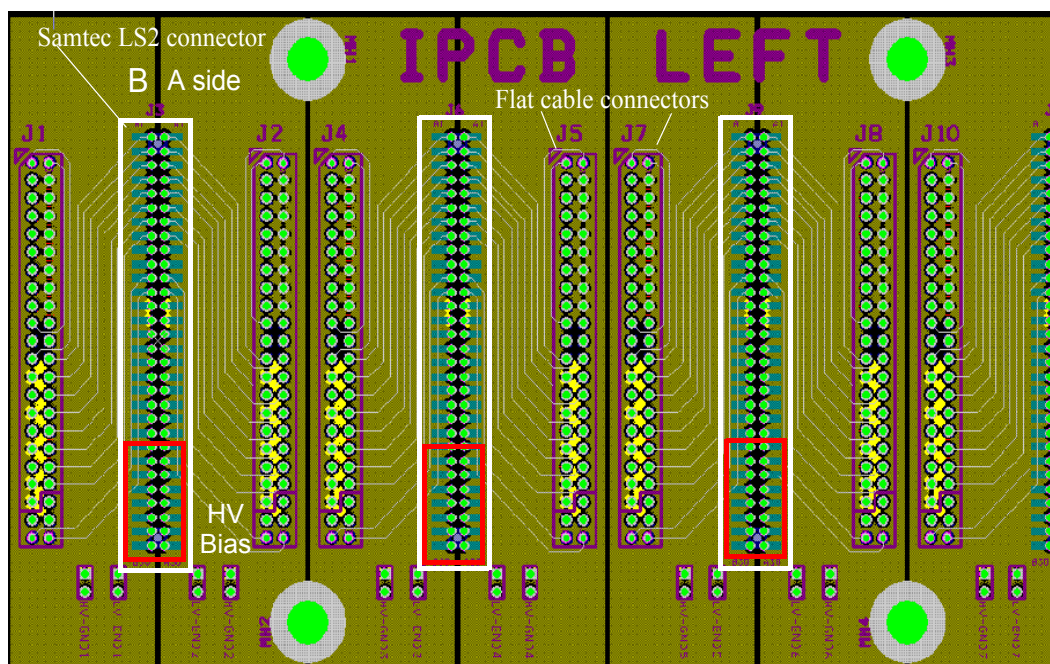


Figure 180 Intermediate PCB for **right side** FEE connectors (referring to Figure 70 and Figure 176 definition of “right”) This corresponds the CSPs (24...31) and (8..15) as shown in Figure 182.



Intermediate PCB for **left side** FEE connectors (referring to Figure 70 definition of “left”) This corresponds the CSPs (16...23) and (0..7) as shown in Figure 182

For laboratory tests, individual IPCB's macros with hand-soldered flat cables have been used. Such test strips can also be obtained by cutting them from a long IPCB strip. The correct connection of such IPCB macros is shown Figure 181 for the upper and lower IPCB and flat cable (40 pin IDC 1.27 mm).

Note: As shown in Figure 181 the AMP connectors (CERN SCEN 09.21.20.130.9) at the end of the flat cables for the T-cards must be rotated by 180 degree respectively for left side (bottom) and right side (top) since the upper/lower T-cards are rotated by 180 degree.

Important: Never confuse left and right IPCB! this can destroy CSPs or FEE cards since their pinout is mirrored.

23.1 Crystal to channel mapping (old T-card)

The CSP numbering in units of 8 is given by octal strip units, which belong mechanically and electrically together. Four strip units, each with 8 CSP grouped via T-cards, are connected via flat cables to two FEE card connectors. Each of the two FEE front connectors connects to two T-cards via flat cables¹. With this, one FEE card defines 32 CSP inputs which are numbered from 0..31. The geographical correspondence between crystals/CSP - T-cards - FEE cards is shown in Figure 182

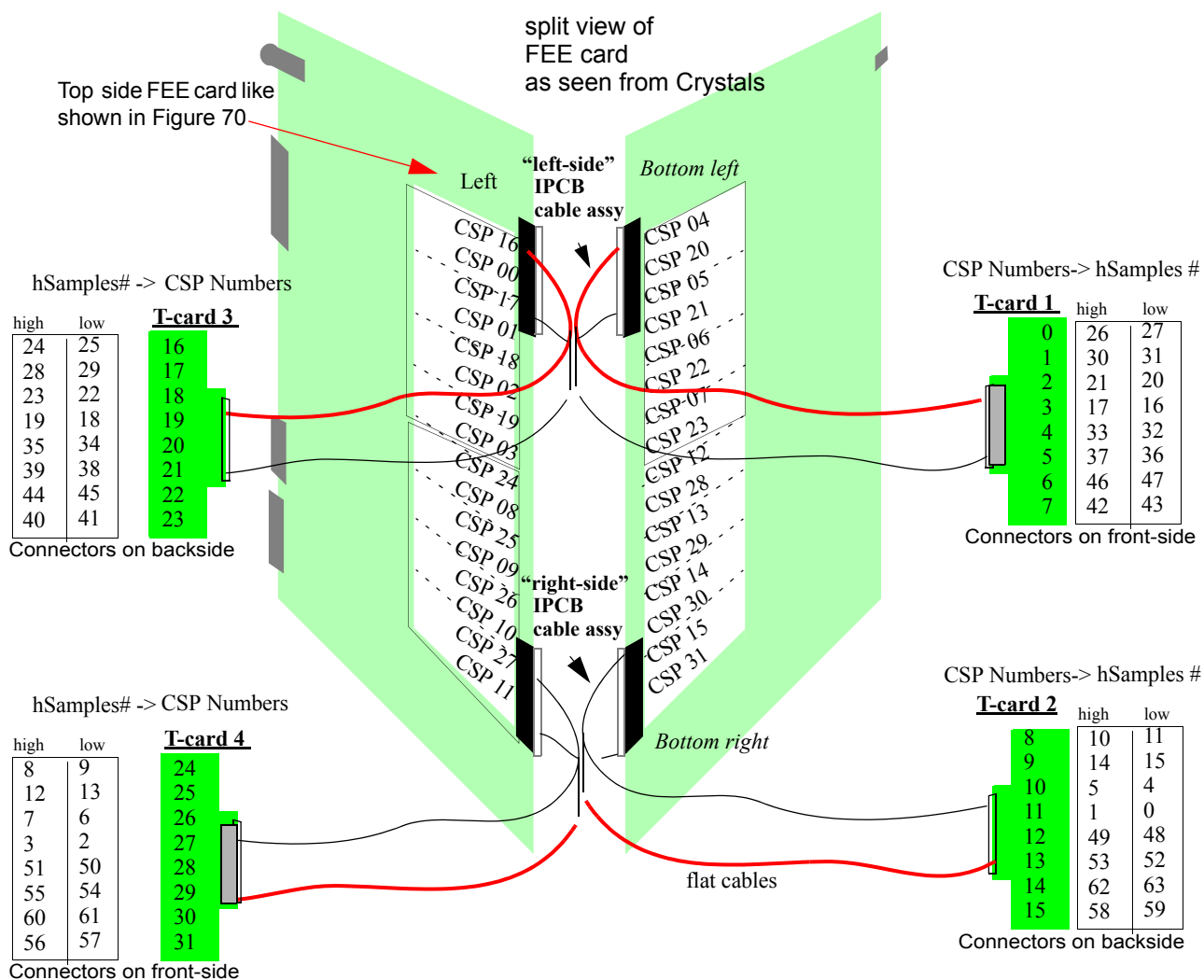


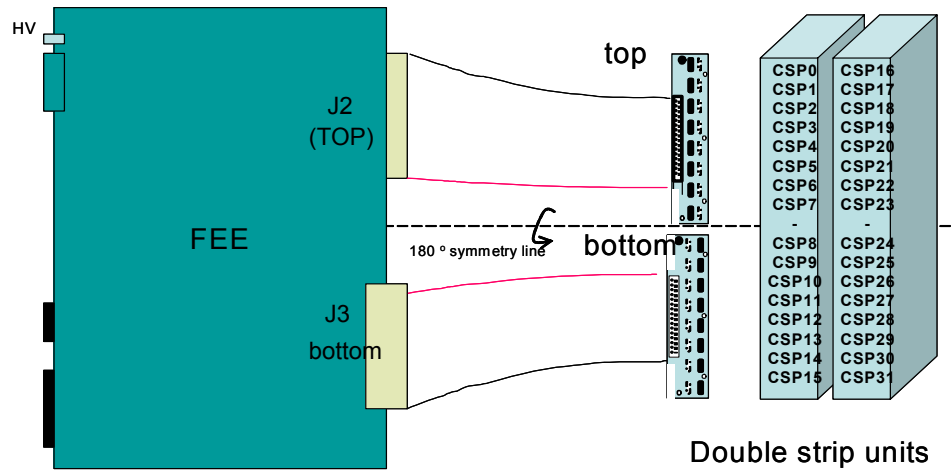
Figure 182 GEOGRAPHICAL position of CSP channels seen from the crystals, on the Top/Bottom sides of the FEE card.

Note: shown next to each T-card is the correspondence with the october 2004 testbeam 'hSample' channels for high and low gain.

1. not shown: PHOS has between FEE connector and flat cable an intermediate pcb (IPCB) as signal router.

23.2 Crystal to channel mapping (new T-card)

The mapping of the new double T-cards corresponds to Figure 182 however there is only one T-card on top



Mapping of CSP channels to FEE Top and Bottom

and bottom.

23.3 Altro channel mapping to CSP

The logical mapping of each crystal/CSP to its two Altro channels (high and low gain) is shown below. This mapping table is ordered by increasing ALTRO addresses, hence does not represent a geographical order.

The CSP numbers are printed on the FEE card shaper inputs and on the HV bias lines.

CSP 0	HI	ALTRO 2	CH 10	CSP 16	HI	ALTRO 2	CH 8	Altro 010b
	LO		CH 11		LO		CH 9	
CSP 1	HI	ALTRO 2	CH 14	CSP 17	HI	ALTRO 2	CH 12	Altro 011b
	LO		CH 15		LO		CH 13	
CSP 2	HI	ALTRO 2	CH 5	CSP 18	HI	ALTRO 2	CH 7	Altro 100b
	LO		CH 4		LO		CH 6	
CSP 3	HI	ALTRO 2	CH 1	CSP 19	HI	ALTRO 2	CH 3	Altro 000b
	LO		CH 0		LO		CH 2	
CSP 4	HI	ALTRO 3	CH 1	CSP 20	HI	ALTRO 3	CH 3	
	LO		CH 0		LO		CH 2	
CSP 5	HI	ALTRO 3	CH 5	CSP 21	HI	ALTRO 3	CH 7	
	LO		CH 4		LO		CH 6	
CSP 6	HI	ALTRO 3	CH 14	CSP 22	HI	ALTRO 3	CH 12	
	LO		CH 15		LO		CH 13	
CSP 7	HI	ALTRO 3	CH 10	CSP 23	HI	ALTRO 3	CH 8	
	LO		CH 11		LO		CH 9	
CSP 15	HI	ALTRO 4	CH 10	CSP 31	HI	ALTRO 4	CH 8	
	LO		CH 11		LO		CH 9	
CSP 14	HI	ALTRO 4	CH 14	CSP 30	HI	ALTRO 4	CH 12	
	LO		CH 15		LO		CH 13	
CSP 13	HI	ALTRO 4	CH 5	CSP 29	HI	ALTRO 4	CH 7	
	LO		CH 4		LO		CH 6	
CSP 12	HI	ALTRO 4	CH 1	CSP 28	HI	ALTRO 4	CH 3	
	LO		CH 0		LO		CH 2	
CSP 11	HI	ALTRO 0	CH 1	CSP 27	HI	ALTRO 0	CH 3	
	LO		CH 0		LO		CH 2	
CSP 10	HI	ALTRO 0	CH 5	CSP 26	HI	ALTRO 0	CH 7	
	LO		CH 4		LO		CH 6	
CSP 9	HI	ALTRO 0	CH 14	CSP 25	HI	ALTRO 0	CH 12	
	LO		CH 15		LO		CH 13	
CSP 8	HI	ALTRO 0	CH 10	CSP 24	HI	ALTRO 0	CH 8	
	LO		CH 11		LO		CH 9	

Figure 183 LOGICAL CSP channel mapping to FEE card Altro chips 4,3,2, 0 channels for high and low gain. (one the PHOS FEE, Altro 1 does not exist !)

The FEE and TRU address correspondence with the geographical numbering of Figure 61) is as follows:

Table 11 RCU address map of FEE and TRU cards (“xxx” is Altro sub-address/registers)

RCU-partition-1		RCU-partition-2		RCU-partition-3		RCU-partition-4	
address	card	address	card	address	card	address	card
0x00xxx	TRU1	0x00xxx	TRU3	0x00xxx	TRU5	0x00xxx	TRU7
0x01xxx	FEE1	0x01xxx	FEE29	0x01xxx	FEE57	0x01xxx	FEE85
0x02xxx	FEE2	“	FEE30	“	FEE58	“	FEE86
0x03xxx	FEE3	“	FEE31	“	FEE59	“	FEE87
0x04xxx	FEE4		FEE32		FEE60		FEE88
0x05xxx	FEE5		FEE33		FEE61		FEE89
0x06xxx	FEE6		FEE34		FEE62		FEE90
0x07xxx	FEE7		FEE35		FEE63		FEE91
0x08xxx	FEE8		FEE36		FEE64		FEE92
0x09xxx	FEE9		FEE37		FEE65		FEE93
0x0Axxx	FEE10		FEE38		FEE66		FEE94
0x0Bxxx	FEE11		FEE39		FEE67		FEE95
0x0Cxxx	FEE12		FEE40		FEE68		FEE96
0x0Dxxx	FEE13		FEE41		FEE69		FEE97
0x0Exxx	FEE14		FEE42		FEE70		FEE98
0x10xxx	TRU2		TRU4		TRU6		TRU8
0x11xxx	FEE15		FEE43		FEE71		FEE99
0x12xxx	FEE16		FEE44		FEE72		FEE100
0x13xxx	FEE17		FEE45		FEE73		FEE101
0x14xxx	FEE18		FEE46		FEE74		FEE102
0x15xxx	FEE19		FEE47		FEE75		FEE103
0x16xxx	FEE20		FEE48		FEE76		FEE104
0x17xxx	FEE21		FEE49		FEE77		FEE105
0x18xxx	FEE22		FEE50		FEE78		FEE106
0x19xxx	FEE23		FEE51		FEE79		FEE107
0x1Axxx	FEE24		FEE52		FEE80		FEE108
0x1Bxxx	FEE25		FEE53		FEE81		FEE109
0x1Cxxx	FEE26		FEE54		FEE82		FEE110
0x1Dxxx	FEE27		FEE55		FEE83		FEE111
0x1Exxx	FEE28	0x1Exxx	FEE56	0x1Exxx	FEE84	0x1Exxx	FEE112

24 Test environment [2]

Basic FEE measurements like single channel noise, linearity, APD gain and shaper timing verification can be made within some limits with oscilloscope and a LED pulser or step pulser. For more precise statistical Root analysis tools for measurement of all channels are to be used (see Chapter 28 .)

Initially, a Philips pulser with 2 ns risetime and signal amplitudes up to 5 Volt was used to generate light flashes with trigger. The APD is directly connected to the CSP preamplifier and powered via a 6 wire-jumper cable from the T-card. With this kind of light pulse generation, timing resolutions of ca. 2 ns were achieved. For a faster light generation, a dedicated nanosecond LED flasher was built to emulate the scintillation light of the PWO crystals. The timing resolution achieved with this type of light generation is so far 1.45 ns.

24.1 Test crate

For testing multiple FEE cards via an RCU and GTL bus branch like in a final experiment, custom test crates were constructed by modifying old Fastbus IEEE 960 crates. The insertion of FEE cards at the same connector

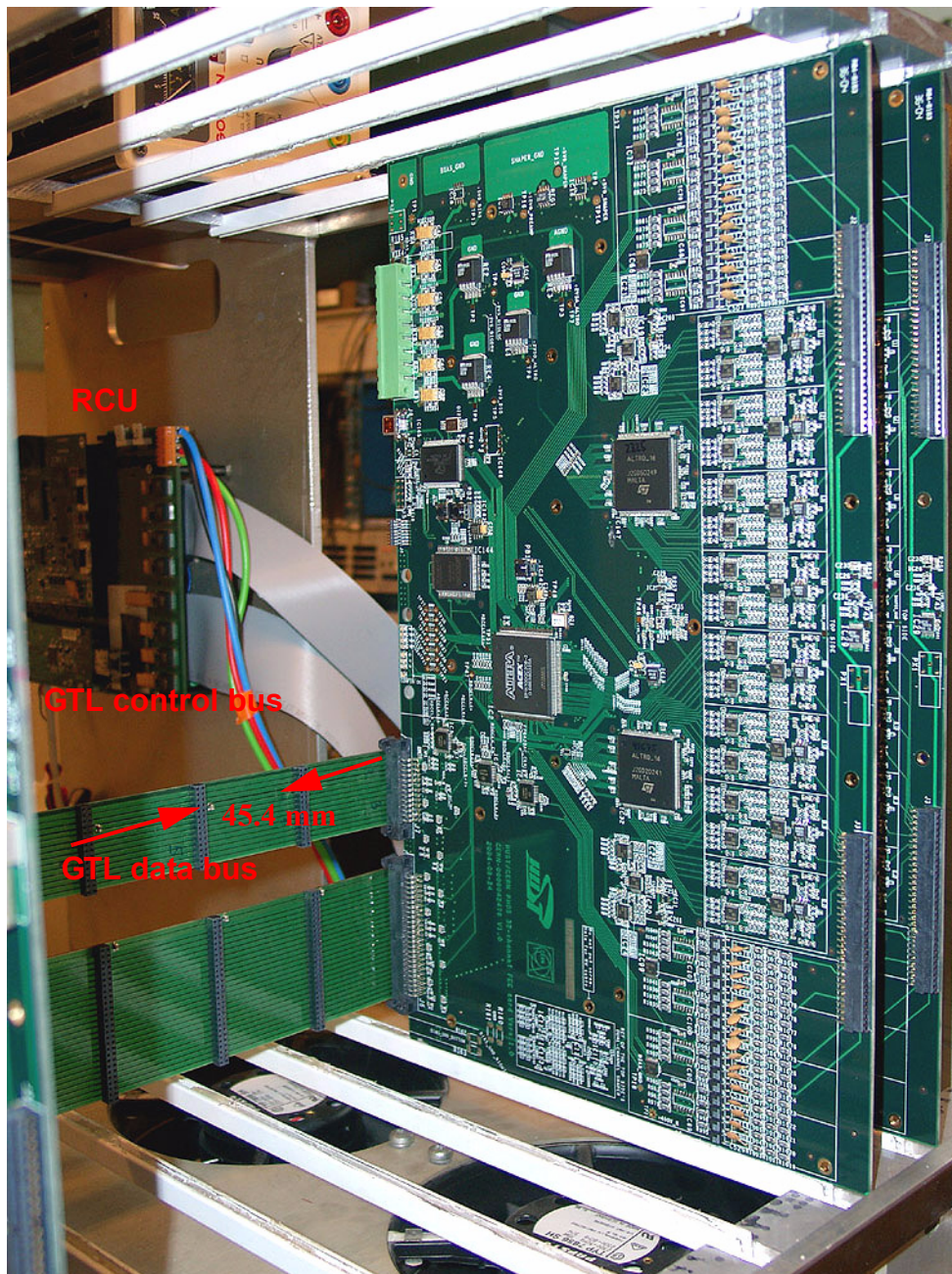


Figure 184 Photo of FEE test crate with two FEE cards.

pitch as two crystals ($2 * 22.7 \text{ mm}$) allows that multiple FEE cards can be tested under the same condition as in the PHOS module.

The references of components for building up a complete FEE test laboratory is listed in Table 23

25 FEE test system

The overview of a full laboratory test system for LED-pulsed FEE tests with RCU and DAQ computer is shown in Figure 185.

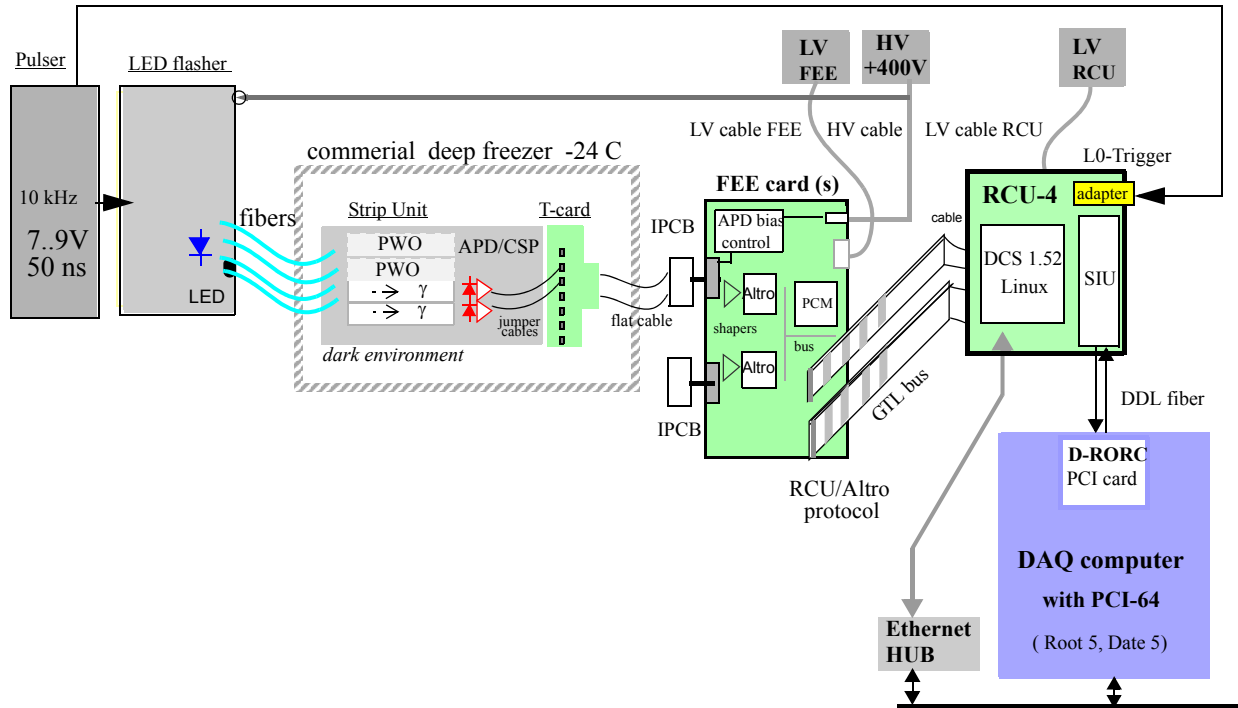


Figure 185 Schematic overview of full test system with Root offline analysis

25.1 High intensity LED flasher

A LED flasher for 470 nm peak wavelength with 1 nanosecond risetime of very high light intensity has been designed by the CERN PHOS team [29] for optical fiber distribution to up to 50 APDs simultaneously.

The principle applied [Figure 186] is that a capacitor is discharged by an avalanche transistor, triggered by an external pulse generator (like TPG 110 from TTI). Prototype measurements are shown in Figure 187

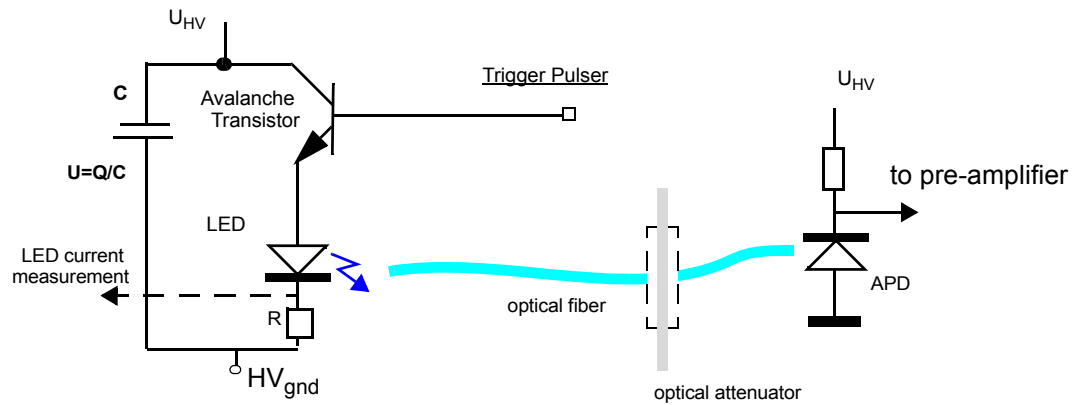


Figure 186 principle of fast LED pulse generation, transmission and attenuation

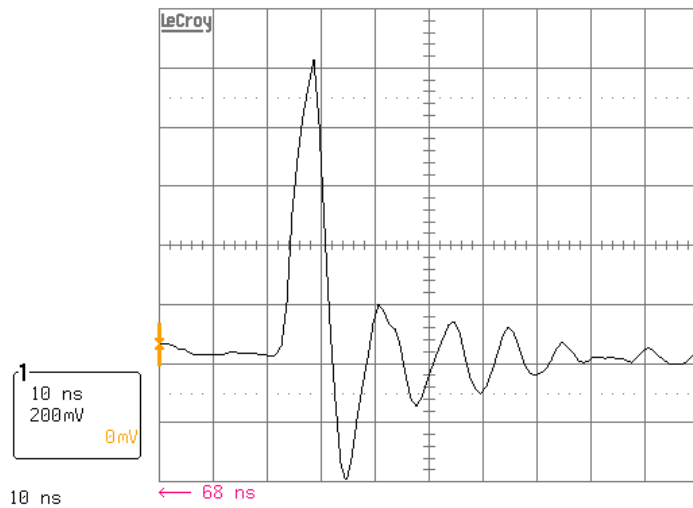


Figure 187 minimal and maximal LED current (voltage at 0.47 Ohm shunt) for different capacitor values. The LED current risetime is 2 ns the peak current 2.5 A.

The current of Figure 187 shows a peak amperage of $1V/0.47\text{ OHM} \sim 2.5\text{ Ampere}$. The LED (Kingbright L7104PCB) is specified for typically 350 milli-candela @ 20 mA. In view that light intensity of LEDs is current proportional, 0.7 mA correspond to ca 44 candela into a light emission angle of 20 degrees. The LED faces



Figure 188 bundle of 8 optical fibers (1mm dia) facing the LED at ca. 2-5 mm distance.

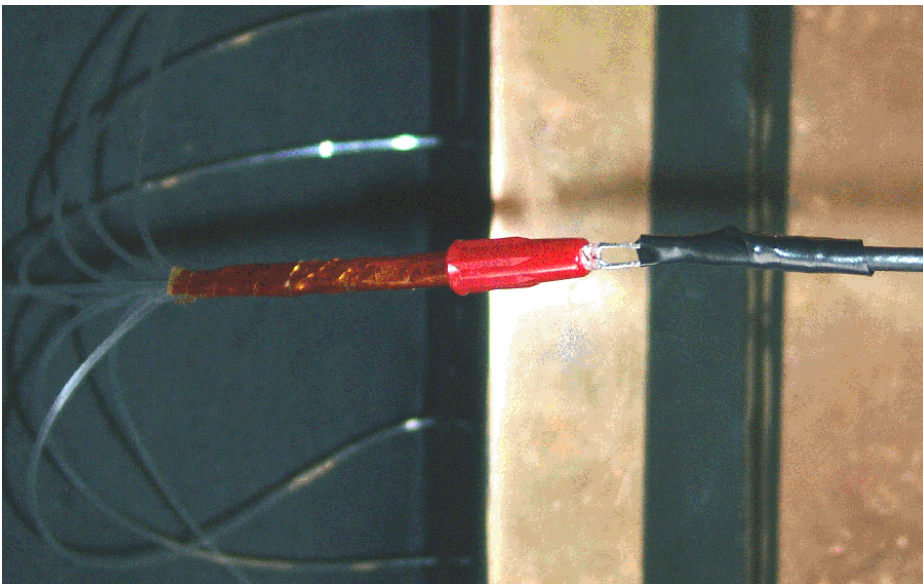


Figure 189 Photo of coupling the fiber bundle via a plastic pipe such that it faces the LED

a bundle of 8 fibers of 1 mm diameter as shown in Figure 188

The blue light flash (470 nm or 2.7 eV photons) of the LED is picked up and transferred over optical fiber of 1mm diameter, to an array of 8 APD/CSP's in a box with Tcard.

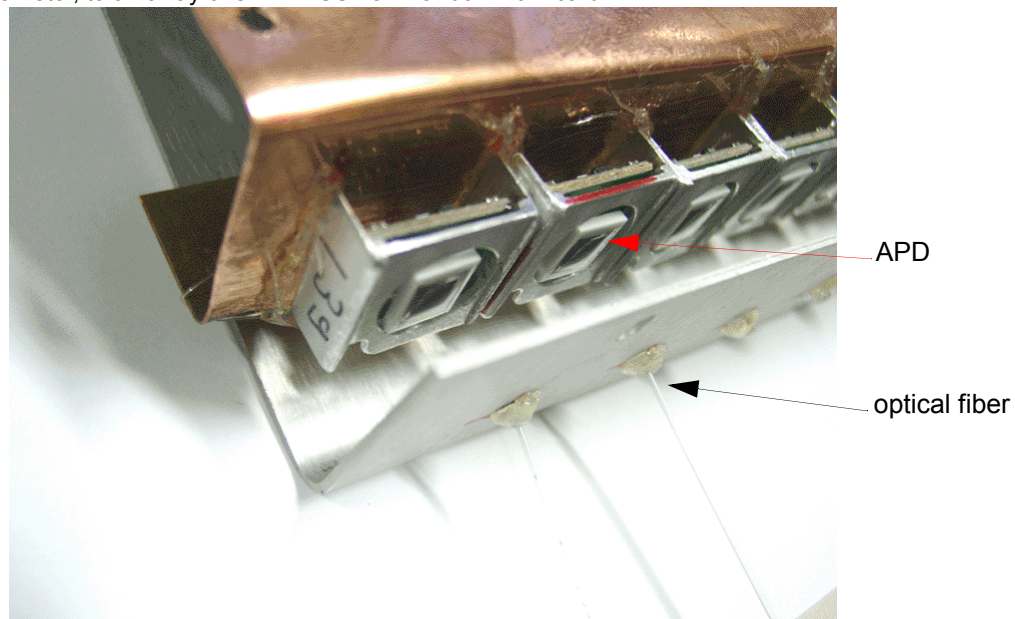


Figure 190 Array of APD/CSP with optical light coupling from a fiber.

The distance of the fiber from each APD can be adjusted by 1 cm, allowing to adjust equal light sharing between all 8 APD's of the test box.

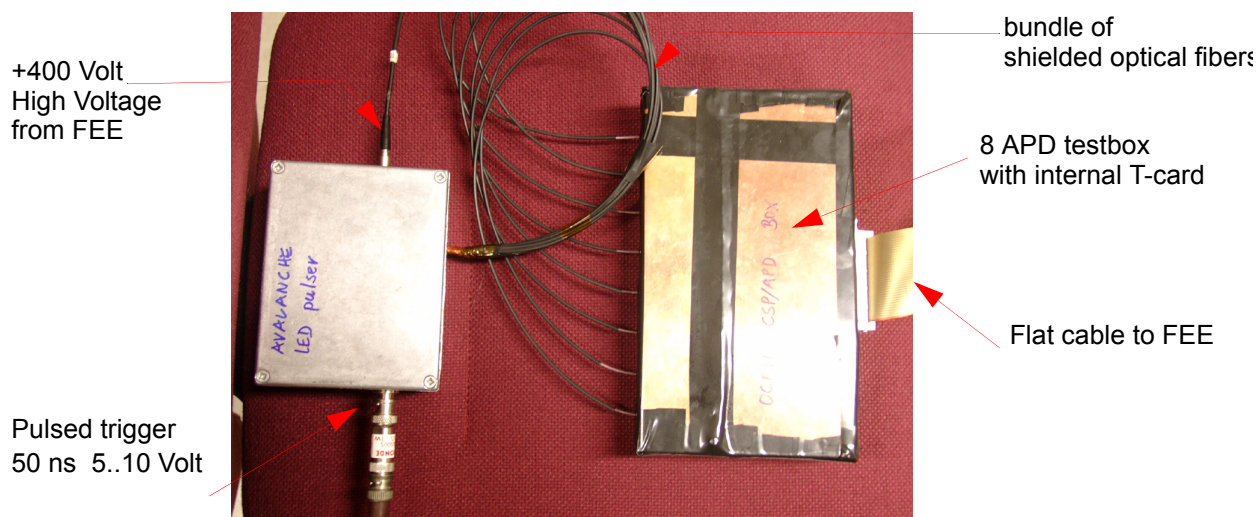


Figure 191 LED pulser box with 8 optical fibers connected to octal APD test box.

The response of the CSP with un-attenuated light easily reaches the overflow of the CSP, at 5 Volt swing (but allows to test the full CSP range with a 1ns pulse).

For the FEE dynamic range (ca 140 mV for high gain and ca. 2.2 Volt for low gain , see chapter 8.7) a light attenuator in form of 1 or two layers of 0.1 mm paper etiquettes on the fiber bundle which faces the LED is sufficient. The CSP response of an attenuated fiber-LED pulse is shown in Figure 192. The CSP risetime is

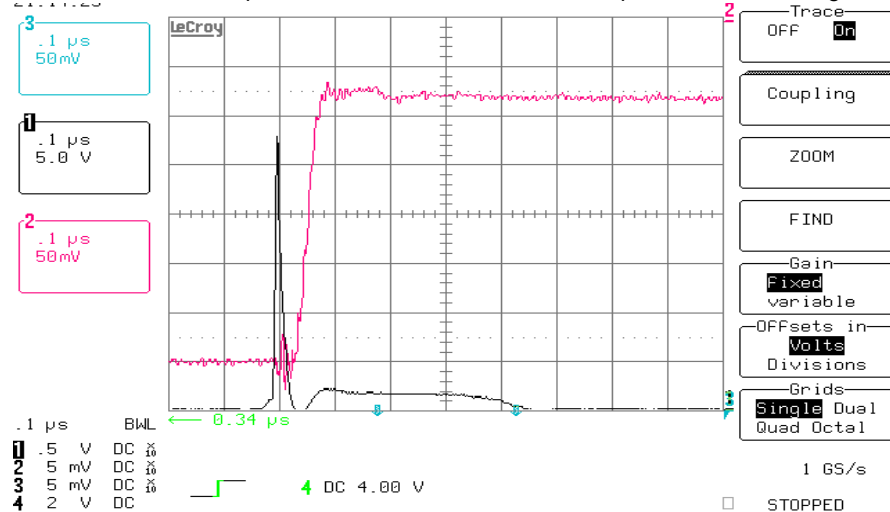


Figure 192 CSP response to a LED flash (Figure 187) transmitted via optical fiber to the APD.

about 30 ns .

Note: if the baseline of the CSP output is unstable (typically 50 Hz variations) it is very probable that the APD is seeing light !

25.2 LED pulser driven by commercial pulse-generator

For single APD tests, a LED can also be driven directly by commercial Pulse generator with 2 ns risetime. A blue Kingbright L-7104PBC LED, connected via 50 OHM coax cable and terminated with 50 OHM (serial resistance of LED + 47 OHM) is used in the test setup shown in Figure 193. Crosstalk between the LED and the CSP is however very difficult to avoid, and the light pulse risetime is not as fast as using the Avalanche pulser. However this method is adequate for generating test CSP step pulses of precisely variable amplitude and with the right dynamical characteristics for the pole-zero compensation circuit of the FEE cards, hence no signal undershoot after the shaper. Note that the light produced is proportional to the LED current,

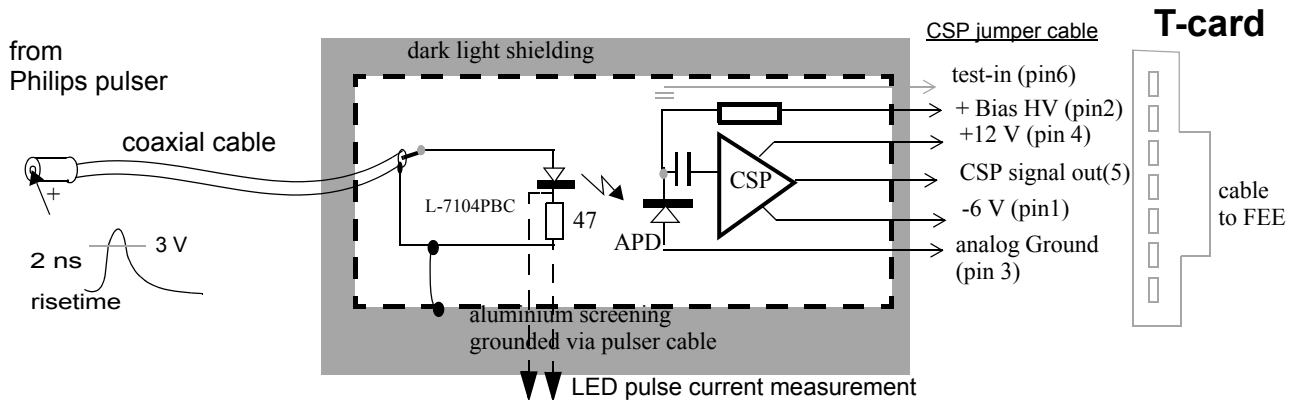


Figure 193 Single channel LED pulser APD test box

The LED starts producing light above ca. 3 Volt.

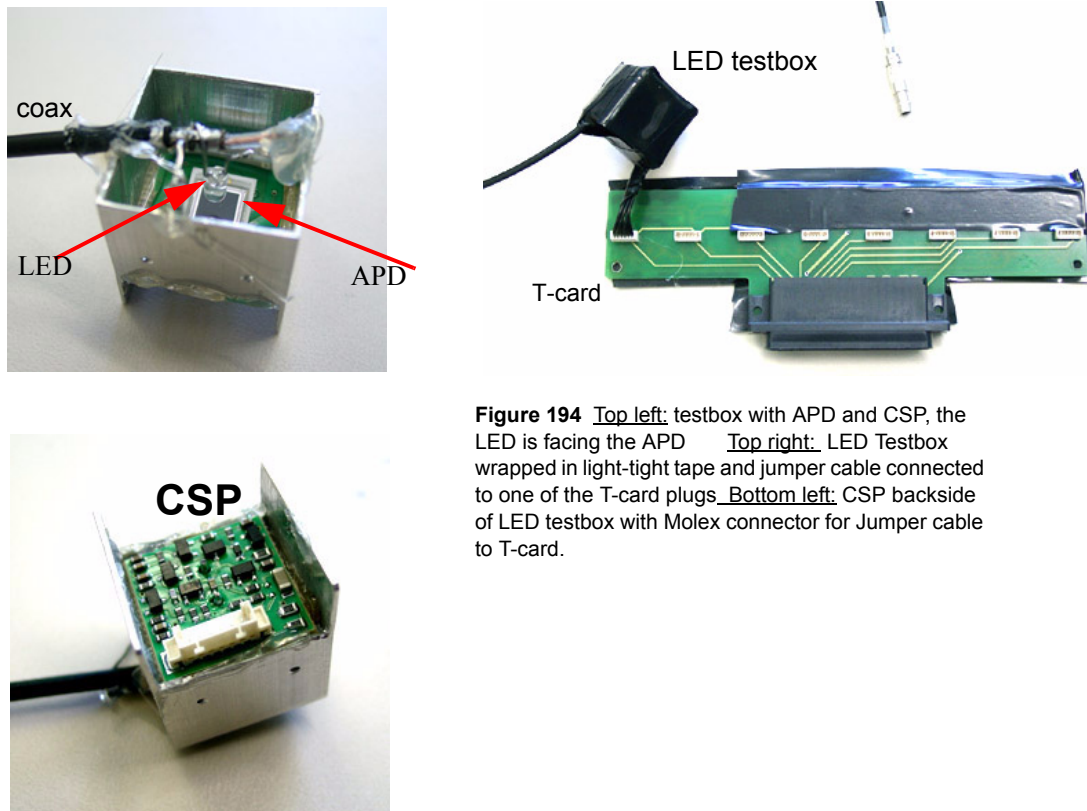


Figure 194 Top left: testbox with APD and CSP, the LED is facing the APD Top right: LED Testbox wrapped in light-tight tape and jumper cable connected to one of the T-card plugs Bottom left: CSP backside of LED testbox with Molex connector for Jumper cable to T-card.

The test setup is connected as shown in Figure 194 . The blue LED faces an APD / CSP assembly inside a small metallic test box which is shielded against light and grounded via the LED pulser cable (not connecting the analog ground of the CSP). The CSP jumper cable connects to one of the eight plugs of the T-card.

The mapping of the chosen channel to the CSP number printed on the FEE cards is shown in Figure 182. All oscilloscope tests should be taken on the FEE card, with ground connected to the analog ground pin in the centre of the shaper area. After finding the corresponding CSP channel at the shaper input, connect the scope probe to:

- a) for measuring CSP output like Figure 192 --- to the corresponding input resistor or capacitor of the shaper.
- b.) for measuring shaper output like Figure 195-- to the corresponding RC output filter after the shaper

For measurements which correspond to the PHOS experiment, the LED pulser APD test box should be placed into a stable temperature environment, this corresponds for PHOS to minus -25 C, i.e the temperature within the deep-freezer compartment of a commercial refrigerator. It is recommended to measure the temperature using a wire temperature probe taped to the APD test box and to note the temperature during data taking. Differences of 1 degree in temperature correspond to -2.2 % of APD gain. Also note down the exact Bias voltage, since 1 Volt difference corresponds of 3% APD gain difference.

Trace the CSP output signal to the shaper input on the FEE card, and then, increase the time scale to 1 μ s / division to see the semi-gaussian output at the output of the shaper (R1145 or R1146) in Figure 164 t

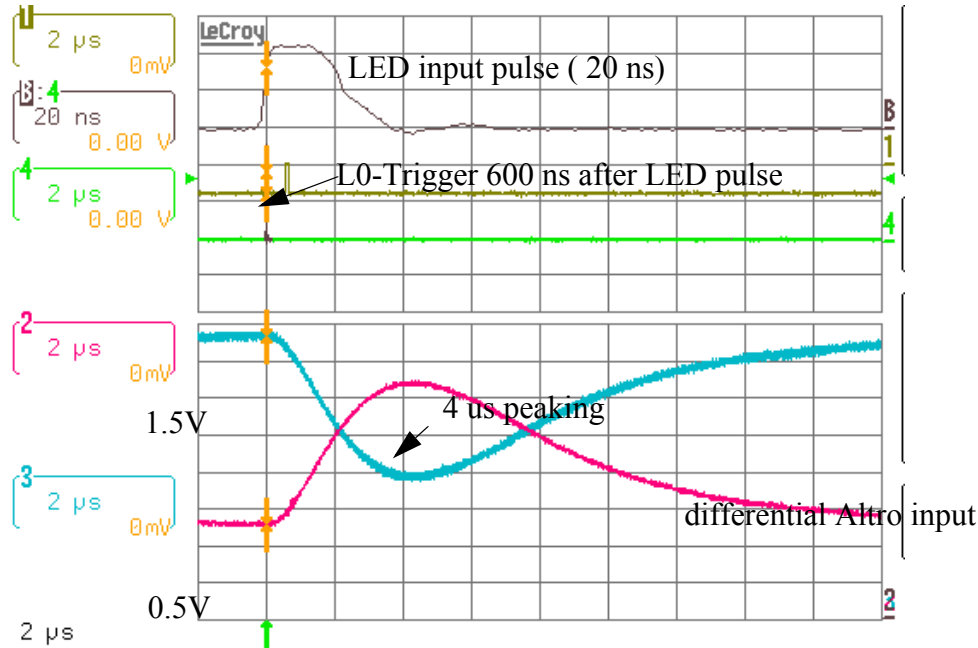


Figure 195 t

typical shaper output at input to Altro digitizer for 4 μ s shaper. The originating LED pulse is shown in a magnified 20 ns time range.

The full timing sequence of LED, shaper and trigger is shown in Figure 195. The delayed L0 trigger signal is generated here 600 ns after the LED is fired.

25.3 CSP step pulse emulation for simple FEE testing

Cheap commercial square pulse generators (like the TGP110 from TTI ¹) can be used for amplitude-variable pulsed testing of FEE channels. This requires an IPCB adapter as depicted in Figure 181 with a signal splitting RC network as shown below in Figure 196. The positive rising edge of the square pulse is used as replacement signal for the CSP signals. The falling edge is to be ignored and the pulse-width should therefore be more than

1. <http://www.tti-test.com/products-tti/text-pages/gen-tgp110.htm>

10 μ s. The max trigger rate to be adjusted on the pulse generator should be 100 Hz. By using the auxiliary TTL sync output with (proper delayed timing) as a trigger for the RCU mezzanine, a simple test setup for testing all FEE channels is available. The relative delay of the test pulse to the trigger pulse should correspond the Level-0 latency in the experiment (approx 1 μ s for PHOS).

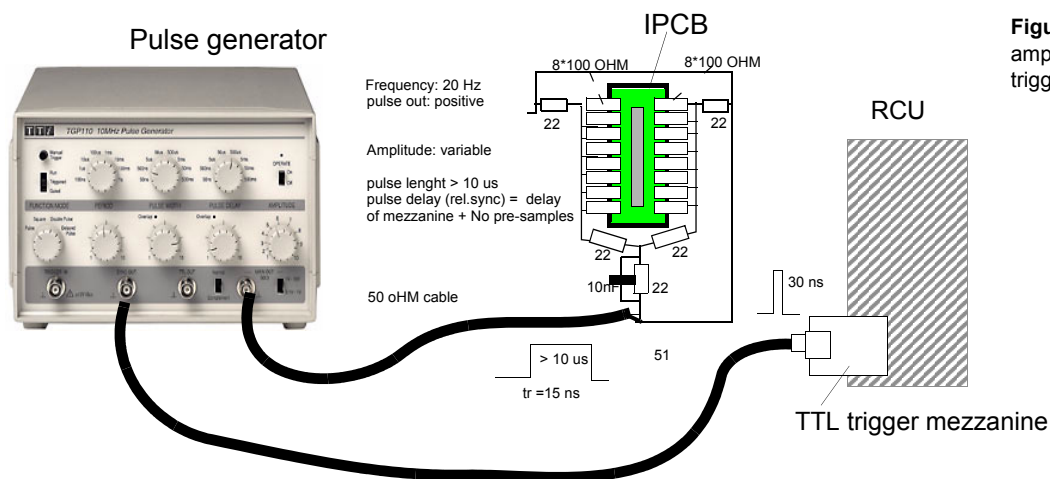


Figure 196 variable amplitude Pulser with trigger to RCU

With artificial step pulses, the CSP signal is overcompensated by the pole-zero network in the input of the FEE cards, hence the shaper-output signals show an overshoot as follows:

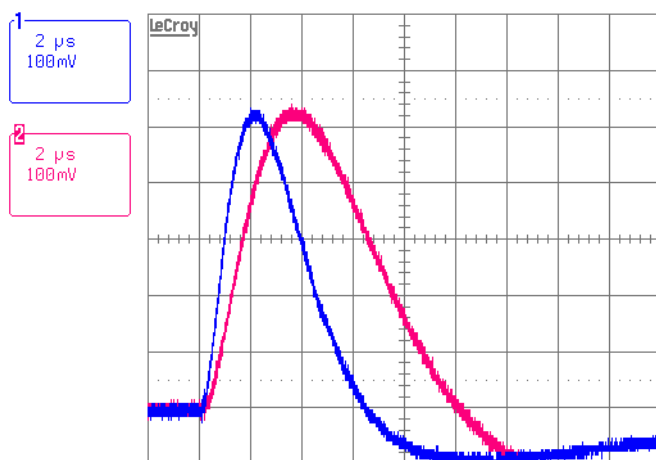
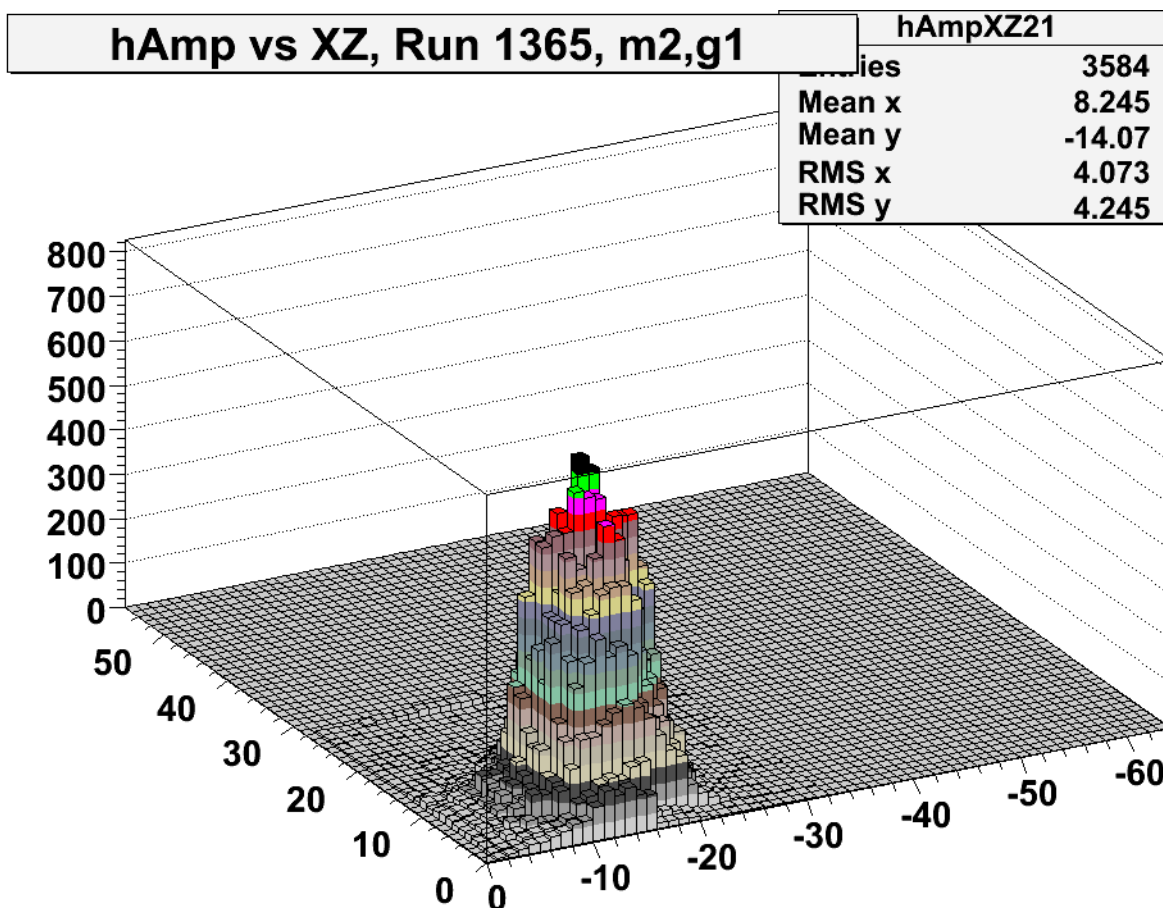


Figure 197 Shaper output signals from artificial step function test input, shown for two peaking times 2 μ s and 4 μ s. The overshoot is due to the artificial test pulses. The offline results obtained in terms of gain and peaking time are therefore slightly different than those obtained with correctly compensated pulses from LED pulsers..

26 Measurement of PHOS characteristics

Figure 198 depicts a measurement taken on one RCU-partition which faces the LED flasher at 1m distance.



2006-07-04

Figure 198 Lego Plot with PHOS of emulated 200 GeV shower generated by the blue LED flasher placed ca 1m on front of PHOS. Note that these data were taken only with very crude APD gain calibration.

26.1 Crosstalk

The light is shared in this test between the two outer, neighboring CSP /crystal channels of an 8-crystal strip unit. This is to simulate real situations and investigate the crosstalk on one strip unit under real load. Crosstalk

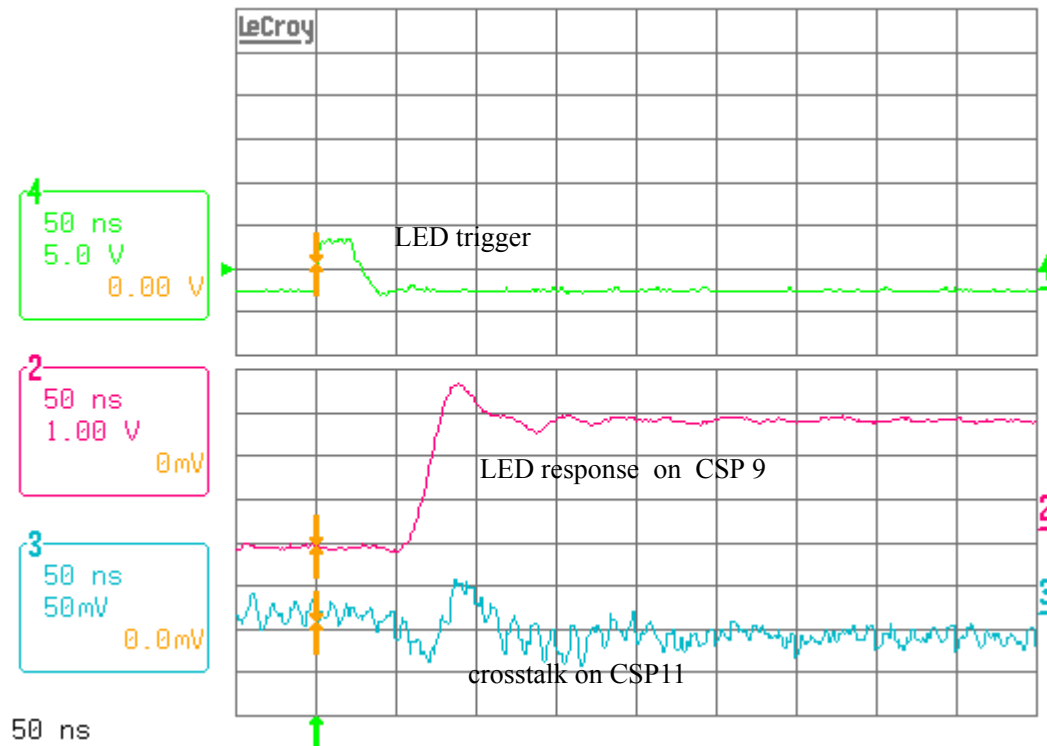


Figure 199 Oscilloscope crosstalk measurement between neighboring channels of one Strip Unit. CSP 9 sees a 3 Volt light pulse, CSP 11 sees no light but measures ca. 50 mV crosstalk

in PHOS is confined mainly to strip units since these are electrically and mechanically operated together.

For example CSP 8,9,10,11..15 belong to one strip unit, connected via a common flat cable. CSP 24,8 or 25,9.. are neighbours only on the FEE card. The above scope measurement shows that the crosstalk between neighboring channels of the same strip unit can be estimated as $50 \text{ mV} / 3 \text{ Volt}$ hence it is a $16 \cdot 10^{-3}$ effect.

27 Readout via RCU

PHOS and EMCal use the same RCU hardware and firmware as the TPC. The connectivity of the GTL readout buses is however different for PHOS and EMCal, also the NIM trigger mezzanine option for level-0 triggers requires the right RCU firmware and proper initialization. The addressing schemes and geographical mapping of the channels are (of course) different for TPC, PHOS and EMCal.

Name	Access	Size	Base Address	Description
AFL	R/W	32bit	0x8000	This register, updated by the Slow Control contains the active front-end card list. The low 16bit correspond to branch A, whereas the higher 16bit correspond to branch B. A bit is set to "1" if a FEC is ON.
RDOL	R/W	32bit	0x8001	
DCSadd	16bit	16bit	0x8007	DCS address field stored in each write transaction
RCU_version	R/W	24bit	0x8008	RCU firmware version
Backplane_version	R/W	1bit	0x8009	TPC (0) or PHOS (1) version for the backplane
TTCclk_freq	R	3bit	0x800A	Frequency of the TTC clk
DCS_ON	W	1bit	0xE000	By executing this command, the DCS card becomes master of the RCU bus. (DCS access only)
DDL_ON	W	1bit	0xF000	By executing this command, the DDL becomes master of the RCU bus. Default condition. (DCS access only)
L1_TTC	W	1bit	0xE800	Enables the L1 trigger coming from the TTC chip
SCLKsync	W	1bit	0x8020	Re-synchronize the SCLK with the next L1TTC trigger
L1_aux	W	1bit	0xF800	Enables the L1 trigger coming from the dedicated connector
L1_CMD	W	1bit	0xD800	Enables the L1 trigger issued by a command (default)
L1	W	1bit	0xD000	Sends L1 trigger if L1_CMD has been previously set
GLB_RESET	W	1bit	0x2000	Resets both RCU and FECs.
FEC_RESET	W	1bit	0x2001	Resets only the FECs.
RCU_RESET	W	1bit	0x2002	Resets only the RCU. It does not affect to the AFL (0x8000) and Backplane_version (0x8009) registers
WRD_RD	W	1bit	0x5xxx	Number of words to be read (in DDL access only)

Table 1.1: Storage and Command Table

Figure 200 Global RCU commands (firmware version > 181206) from <http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc/firmware.htm>

Figure 200 depicts the list of global RCU commands, like the backplane version which must be set to PHOS=1 for the PHOS detector.

27.1 Readout Control Unit (RCU)[18]

The Readout Control Unit of the TPC project is also the Readout Bus master of PHOS FEE cards. It is an FPGA based protocol interface between the DCS or SIU and the FEE cards. The firmware is slightly different than the TPC firmware due to different geographical address mapping of PHOS (compare Figure 105). Each RCU partition consists of two GTL bus branches (A , B), each containing 14 FEE and 1 TRU card. Each GTL bus interconnects the RCU with 14 FEE cards and 1 TRU, hence one RCU readout partition consists of 28 FEE cards and 2 TRU cards, covering 1/4 PHOS module with 12*32 crystals. The Linux subsystem on the DCS mezzanine card allows the user to set up all FEE readout modes inclusive the trigger modes via a command

and register interface, defined in the RCU manual via specific base addresses and command functions [24]. The corresponding hardware-level control language (DCS scripts) can be executed within Linux RCU-shells on the DCS card (see chapt. 30). The data transfer to the DAQ computer requires a bi-directional DDL link, interface via the SIU mezzanine.

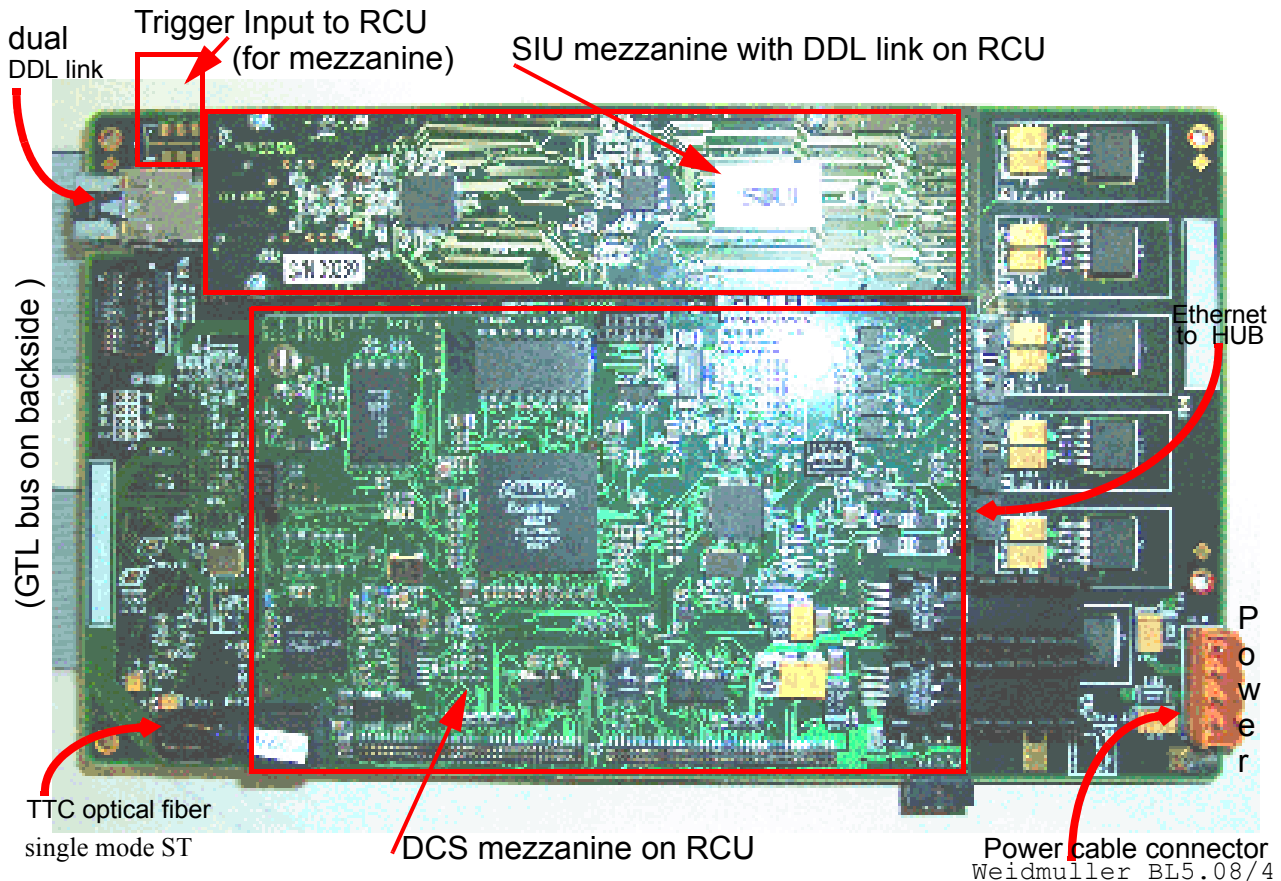


Figure 201 Photo of the new RCU-4 equipped with DCS and SIU mezzanine cards.

27.2 RCU Trigger input mezzanines

For generating an external level-0 trigger for the RCU readout, a secondary output of a test pulser or a TTL signal may be used. Note that in the experiment, the level-0 trigger signal of the TTC fiber can be used, hence these trigger mezzanines serve mainly for test environments.

- 1.) 50 OHM NIM signal of 100 ns with NIM input mezzanine card
- 2.) High impedance (TTL) signal as trigger for a monostable with trigger delay tunable via a potentiometer

The level-0 timing is to be generated according to the trigger presampling initialization see 3. for an Altro-pre-sampling pipeline of max 14 * samples

Enable the trigger:

w 0xf800 0x1 enable mezzanine card trigger on S2 (FPGA input pin G18)

The trigger from the mezzanine must get enabled via the L1_aux register at 0xf800, in case the trigger comes from the TTC, it has to get enabled correspondingly via the L1_TTC address at 0xE800

27.3 RCU address scheme

The 20 bit RCU addressing scheme for DCS broadcast or buffered write instructions to FEE resources (Altro or PCM), based on RCU address decoding is depicted in Figure 202.

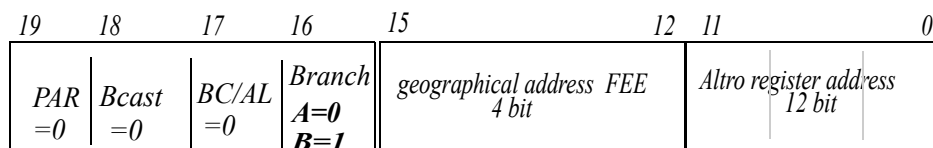


Figure 202 RCU address decoding

27.3.1 NIM trigger input mezzanine

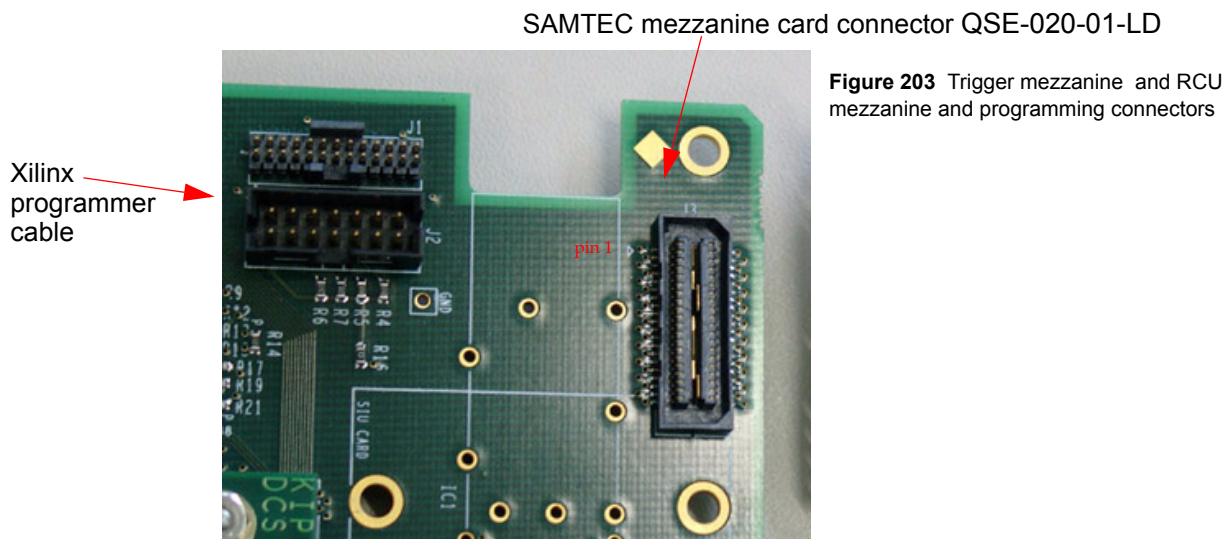


Figure 203 shows the SAMTEC (QSE-020-01-LD) connector corner on the RCU on which a level-0 NIM signal

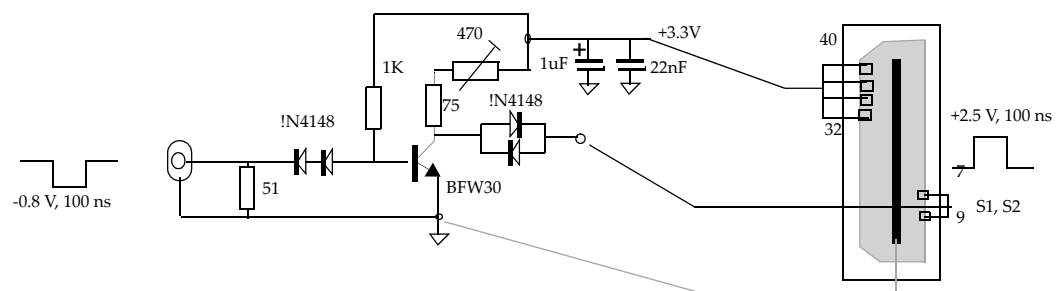


Figure 204 NIM-> LVTTTL prototype converter

input adapter [21] is to be plugged (see Figure 205) . Note that the connector has the middle bus bar connected

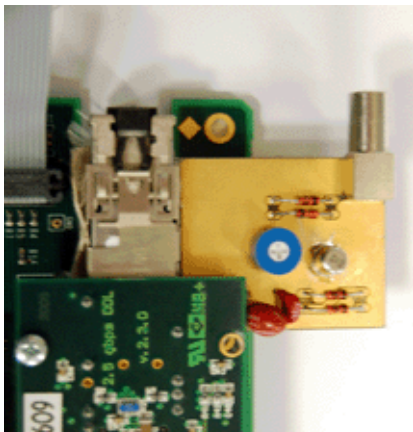


Figure 205 Photo of trigger mezzanine (L0) for NIM signal plugged to the RCU connector

to the RCU ground. The mating connector on the mezzanine card is: QSE-020-01-LD. The RCU mezzanine

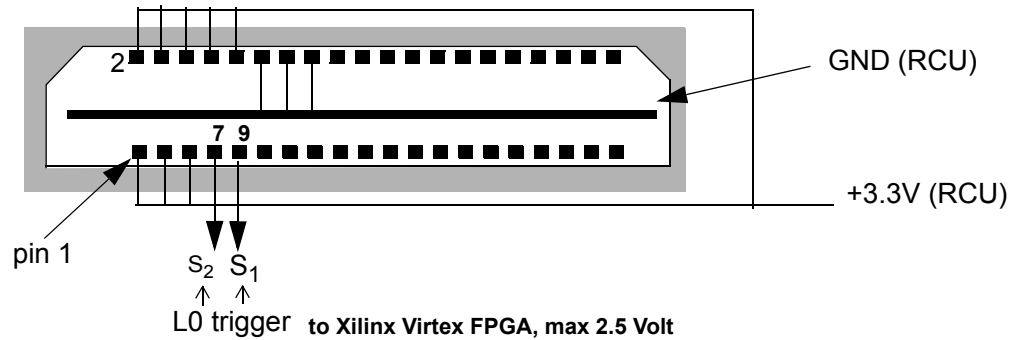


Figure 206 Pinout of Samtec trigger corner connector on RCU

corner connectivity is shown in Figure 206.

27.3.2 TTL trigger signal input

For TTL triggers, the schematics of Figure 207 shows how a 1kOHM impedance clock input from a pulse generator with adjustable delay can be connected

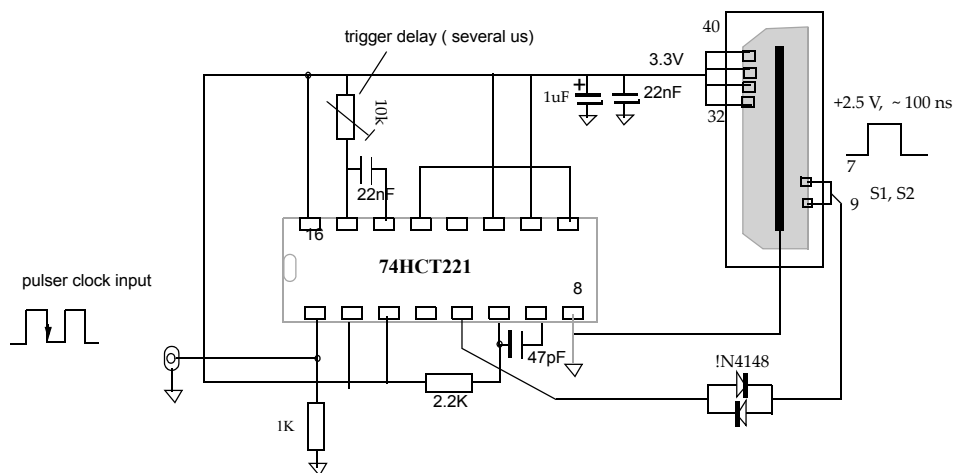


Figure 207 Schematics of TTL mezzanine with adjustable monostable delay

An adjustable delay of several μs can be generated on the mezzanine card at the falling edge of the input pulse (schmitt trigger input). At the end of the (adjustable) delay, a LVTT pulse of 200 ns duration and 2.5 Volt amplitude is sent to the trigger input of the FPGA on the RCU.

27.4 RCU bus protocol [3]

The RCU bus protocols have some similarity with the Fastbus protocols of the LEP era: geographical addressing via a handshake bus protocols, some CSR registers for Control and Status and DMA from the devices (Altros) towards the readout controller (RCU). The latter is the CHRDO protocol which has to be set up via readout list in the RCU. When the RCU gives a CHRDO command to an Altro, the Altro asserts the Transfer TRSF signal and starts sending 40 bit data words, each one being validated by the DSTB strobe. The Altro commands sent by the RCU are:

- WPINC (increase the write pointer)
- RPINC (increase the read pointer)
- CHRDO (channel readout)
- SWTRG (Software trigger)
- TRCLR (Clear Trigger counter)
- ERCLR (Clear Error)

When a command is sent, the RCU asserts the CSTB until the Altro acknowledges the command by asserting ACK*.

These basic protocols can be verified via an oscilloscope or logic state analyzer connected on the GTL bus.

For measuring the 40 bit Altro-RCU protocols, scope-probes should be connected to one of the GTL Control bus connectors. The pinout is viewed on the GTL strip is depicted here. Note however that the two bottom and top connector holes are not populated ! The counting of pins starts above the empty holes

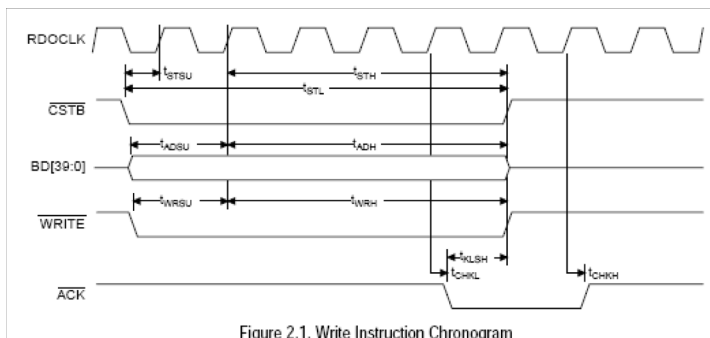
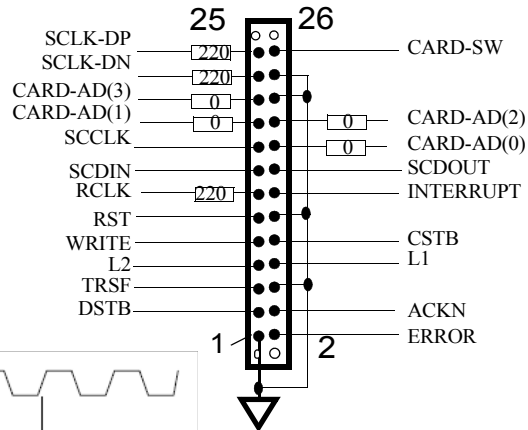


Figure 2.1. Write Instruction Chronogram

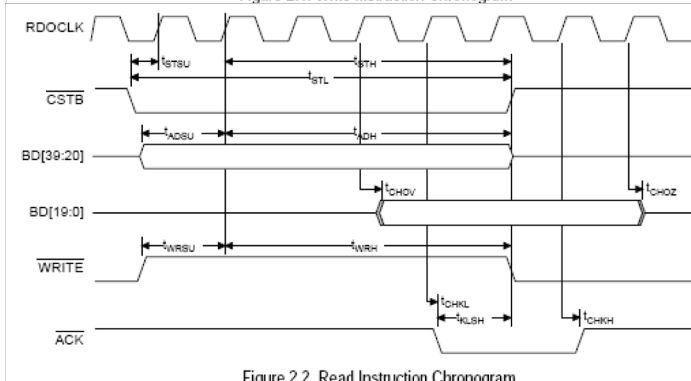


Figure 2.2. Read Instruction Chronogram

Figure 208 Basic Read/Write Chronograms of the RCU/FEE control bus , for details see Altro manual.

CHRDO block transfer chronogram (Altro data transmission to RCU)

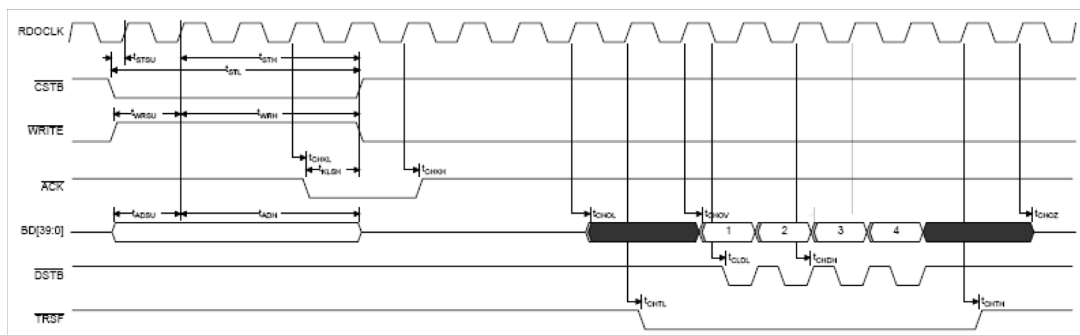


Figure 209 shows the GTL bus write protocol measured via scope probes on GTL bus

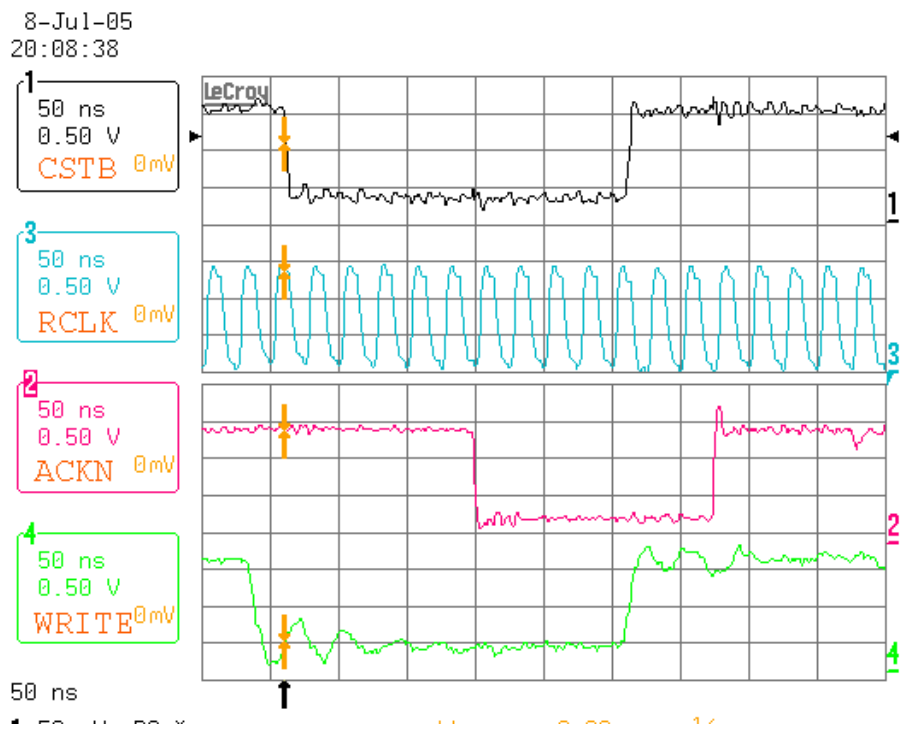


Figure 209 Standard write chronogram between RCU and FEE card.

CHRDO protocol (Altro is DMA bus master during TRSF)

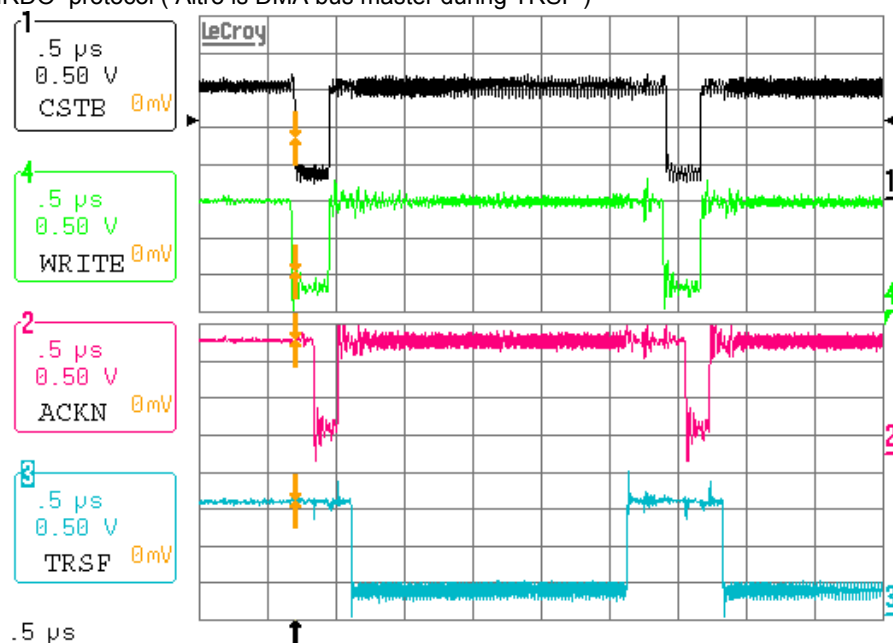


Figure 210 Read instruction chronogram: the Altro becomes bus master during TRSF

In Figure 211 the RCU requests from each Altro (CSTB* -ACKN*) the CHRDO transfer (TRSF signal). During

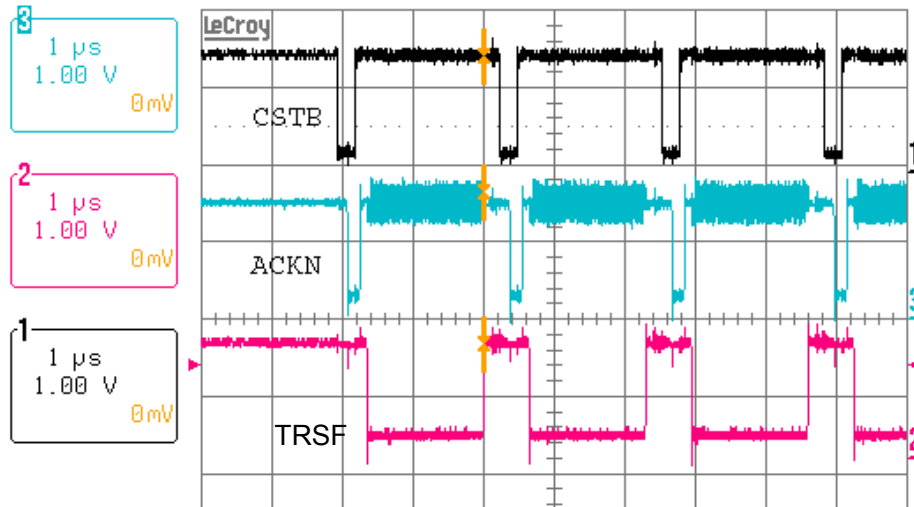


Figure 211 RCU-controlled series of readout commands (see 3.) to readout all Altros in the readout list. Each TRSF frame transfers here 308 Altro samples of the selected channel.

TRSF, the Altro sends all its buffer contents.

In a triggered readout (Figure 212) the RCU starts the readout after the L2 trigger. In software controlled trigger mode 2, the RCU generates L2 after a programmable clock delay after L1 (see TW parameter in 30.9)

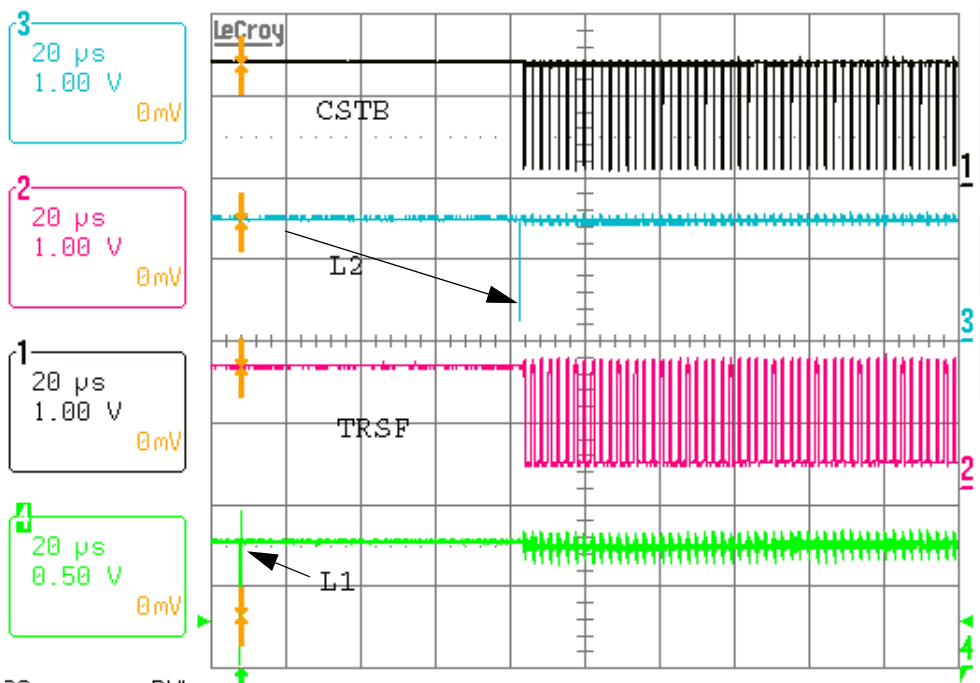


Figure 212 CHRDO readout block after Level-1 and Level-2 trigger pair

28 Offline evaluation methods and results

Statistical measurements like Pedestals, RMS noise, peaking time, high/low gain ratio and differential timing resolution can only be reasonably performed with statistical analysis methods which accumulate a lot of data from all channels. The Root Macros are the most powerful method for accumulating and sorting a large number of data in histograms defined by the user. Root is also the analysis tool to be used in the experiment.

28.1 ROOT evaluation macros

The single shape plots in Figure 46 are obtained via the ROOT Macro:

shape.C(runNumber, cspChannel, highLowGain, xMin, xMax, pedX1, pedX2)

where *runNumber* is the run number and *cspChannel* is the CSP channel, *highLowGain* is 1 for high gain channels, *xMin* and *xMax* are fit range values in ADC samples, *pedX1* and *pedX2* are the range values in pre-samples.

On top of single event shapes, a set of Root Macros were developed for measuring simultaneously all of the initialized readout channels of the FEE card. The fitted single event values are channel-wise accumulated into summary histograms like Figure 46 allowing to obtain the statistical characteristics of all FEE channels in single run representations. As an example

get_TauAll.C(runNumber)

obtains the statistical peaking time t_{Amax} for all 32 channels of an FEE card. The macros are used to obtain:

- pedestals
- RMS noise levels
- peak gains and H/L gain ratios
- shaper peaking time
- Higher level summary histograms display the summary values over all channels per FEE card.

28.2 Offline fit parameters

The Gamma-2 fit shown in Figure 46 is based on ADC data taken with a sampling frequency of 10 MHz, the signal envelope is measured here by 240 samples of 100 ns (including 15 pre-samples) counting from the arrival of the external L0 trigger signal. The peaking time is 20 samples = 2 us.

The pre-sampled area is important for pedestal and RMS determination, in particular since during presampling no digital noise is generated by the ADC. The L0 trigger timing, the ADC pre-samples (max 14) and the sampling rate must be chosen such that sufficient pre-samples (min. 8) precede the signal.

- The Xmax range of the fit is taken at ca 1/3rd amplitude after tmax. In this way the Gamma function represents very well also the pedestal presamples¹.
- The Xmin range of the fit must include the pedestal presamples
- The pedestal pre-samples are used to determine the pedestals and pedestal noise before a pulse. Hence for best results the interest is in advancing the trigger and/or initialize the Altro to the maximum number of pre-samples.
- The amplitude-independent point of the maximum slope ($y'=0$, $y''=0$) are the reference points for timing measurement

The falling slope is very critically connected with the pole zero cancellation input stage of the CW shaper, i.e should not be considered as 100% compliant with the Gamma function. The pole zero network returns the signal to zero without long-timeconstant under- or overshoot. This feature is of benefit for peak amplitude linearity, for reduced pileup error and it preserves proportionality between charge and peak amplitude.

Though evaluation results here show the full envelope of the shaper pulses, for data taking the falling tail recording does not contain much information and can be discarded for the benefit of lower readout bandwidth.

28.3 Shaper gain ratio

Gain factors for the high gain channels relative to low gain channels are obtained by taking the ratio of the resulting amplitudes of ALTRO samples from the gamma-2 fit. The following plots are results by executing a Macro:

.x get_AmpAll.C(runNumber)

1. the falling slope deviates with increasing time from the Gamma Function

Figure 213 below shows the gain ratio of High/low gain of all 32 FEE channels.

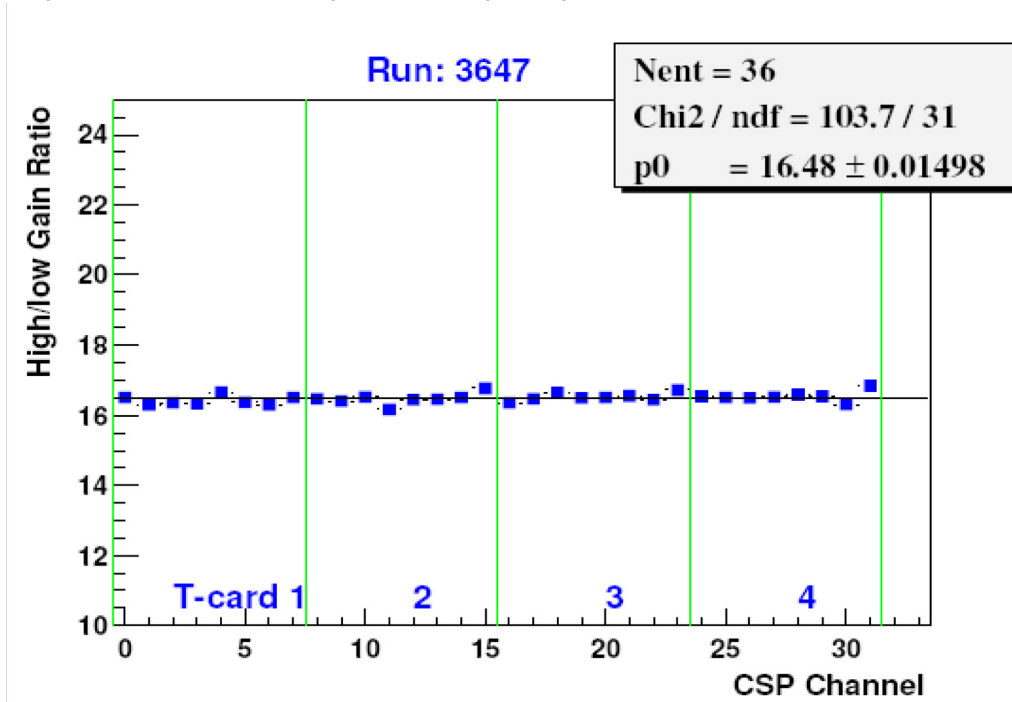


Figure 213 Gain factors of high gain over low gain for a 2 us FEE card.

28.4 Timing resolution

The differential timing resolution can be measured offline by taking the statistical difference of from 2 channels which share equal light of the same LED source, or from the same step pulser (Figure 47). The latter measures the timing resolution of the FEE card alone.

The ROOT macro to retrieve the timing resolution histogram from ROOT files is:

.x seeHistoNxM.C(runNumber, "hRiseTimeDiff", cspChannel, highLowGain)

The timing resolution obtained with this method as sigma of the distribution is to be corrected by $\sigma/\sqrt{2}$ since one channel is measured against the other one, and the timing solution of both channels is assumed equal.

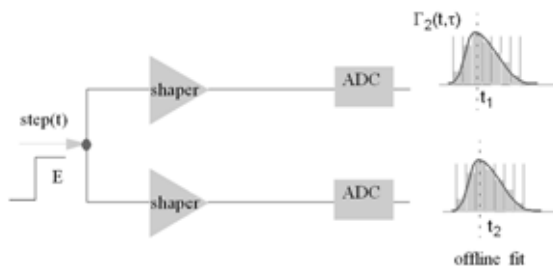


Figure 214 Principle of differential timing resolution measurement, here shown with STEP function input

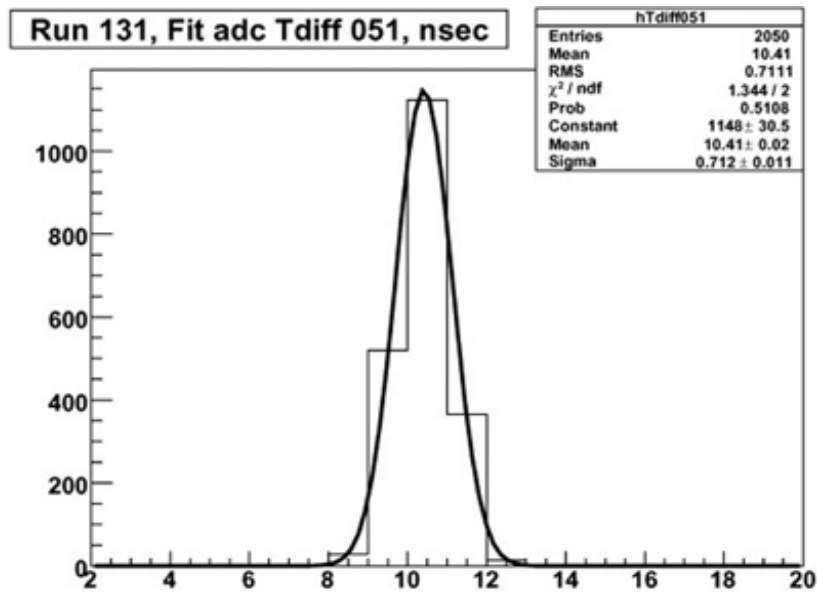


Figure 215 Timing resolution High Gain of FEE card with step pulser $0.712/\text{SQRT}(2)=0.5 \text{ ns}$

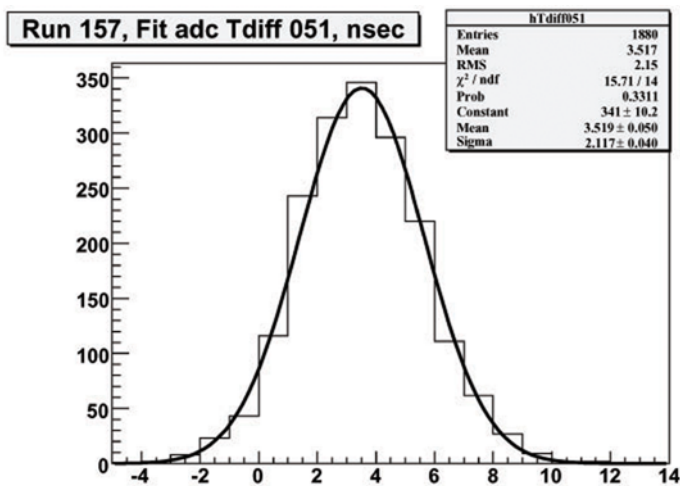


Figure 216 Timing resolution HG with LED pulser and APD @ M=50 $2.117 \text{ ns}/\text{SQRT}(2) = 1.5 \text{ ns}$

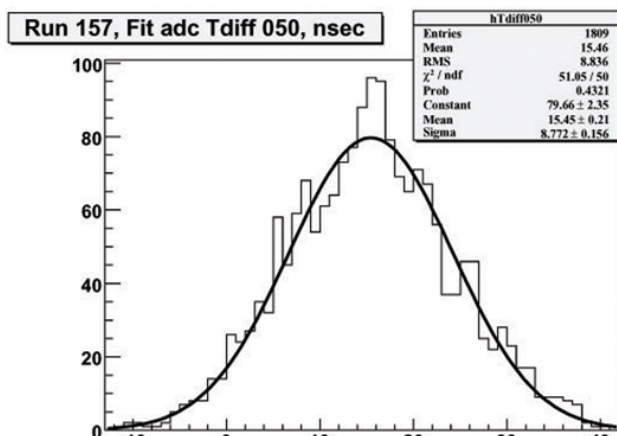


Figure 217 Timing resolution LG with LED pulser and APD @ M=50 $8.77 \text{ ns}/\text{SQRT}(2) = 6.2 \text{ ns}$

By combining the timing resolutions of High Gain and Low Gain, the result obtained is 1.45 ns.

These measurements refer to an equivalent channel energy of 2 GeV (pedestal-corrected ca. 400 peak ADC counts of Run 157 see Figure 46). The 1/E energy dependence of the timing resolution for offline measurements with 10 bit ADCs was already discussed in chapter 1.5

29 Root Macros of 2004 testbeam [12]

A number of Root Macros were developed¹ for the first FEE card test in october 2004. Examples are:

shape.C (), mpsee.C (), see8.C (), getRMS.C (), mpseeADC ()

After recording a run of Number xyz, the xyz.raw data are to be accessed by root and converted in root spectra via:

```
root[3] run.C(xyz)
```

A useful display of shaper signal output in a canvas of size NxM within a range of 2 FEE cards is possible with the root Macro

mpseeNxM.C (runNumber, "hSamples", High/Low, row, column, x, y)

where "hSamples" is a name for all 64 histograms

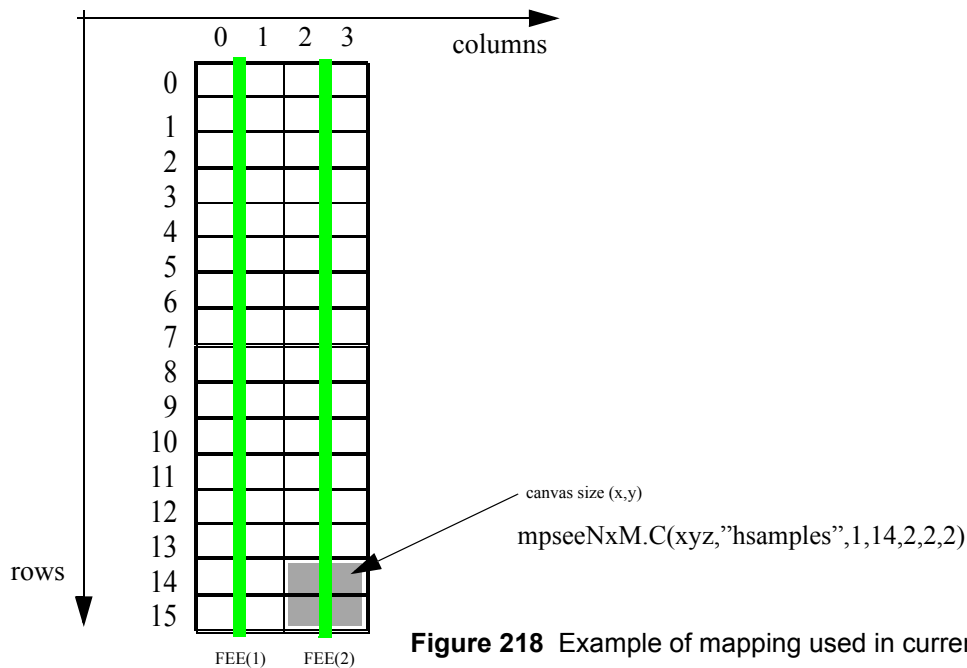


Figure 218 Example of mapping used in current Root Macros

The High/Low selector argument is 1 for display of high gain channels and 0 for low gain channels, the row and column argument designate the position of the display window within the 2*16 crystal matrix, with x and y giving the dimension of the displayed histogram canvas. The CSP-to-Root histogram channel mapping used in the october 2004 testbeam for two FEE cards is shown in Figure 218.

1. written by A.Kouriakine

There are 32 high gain channels (Table 12) and 32 low gain channels (Table 13), in total 64 histogram channels are generated

Table 12 geographical CSP -to- Root histogram channel mapping (32 HIGH Gain channels)

CSP	hSample histogram Nr High gain		CSP	hSample histogram Nr High gain
left side Figure 182			Bottom left sideFigure 182	
	24			33
0	26			35
17	28			37
1	30			39
18	23			46
2	21			44
19	19			42
3	17			40
right side Figure 182			Bottom right side	
	08			49
8	10			51
25	12			53
9	14			55
26	07			62
10	05			60
27	03			58
11	01			56

Table 13 geographical CSP -to- Root histogram channel mapping (32 Low Gain channels)

CSP	hSample histogram LOW gain		CSP	hSample histogram Low gain
Top-right Figure 182			Bottom left Figure 182	
16	25		4	32
0	27		20	34
17	29		5	36

Table 13 geographical CSP -to- Root histogram channel mapping (32 Low Gain channels)

CSP	hSample histogram LOW gain		CSP	hSample histogram Low gain
1	31		21	38
18	22		6	47
2	20		22	45
19	18		7	43
3	16		23	41
Top=-left Figure 182			Bottom right	
24	09		12	48
8	11		28	50
25	13		13	52
9	15		29	54
26	06		14	63
10	4		30	61
27	02		15	59
11	0		31	57

In the following test, a single strip unit with 8 CSP channels was connected to T-card 2 (Figure 183) One common LED pulse was applied to neighboring 2 CSP channels (CSP 8 and CSP9).

The selected channels are displayed in their geometrical position by the root macro mpseeNxM in a matrix of 4*16 crystals which corresponds to 2 FEE cards or 4 parallel crystal columns of 16.

Figure 127 shows a subset of the matrix, a x=2, y=2 Root canvas, anchored at the bottom (x=14) of the high gain channel column. This result was obtained by execution of the root macro mpseeNxM with the following arguments:

```
root[0] .x mpseeNxM.C(3273,"hSamples",1,14,2,2,2)
```


30 Diagnostic DCS scripts and commands [24]

Memory mapped hardware instructions for RCU, FEE and Altros are executed within a dedicated Linux shell (rcu-sh) of the DCS card, after it has been enabled to become RCU bus master. Full details on DCS syntax is given in the RCU firmware: "registers and commands" manual and the Altro User manual [3]. Single commands can be grouped in scripts which are normally used to initialize the RCU readout system, to configure the PCM registers of the FEE cards to execute commands.

Standard DCS scripts used for FEE card testing are:

init	resets the DCS/RCU/FEE chain
get_serial_no_sx	read and display the serial number of card in slot x (below Figure 114)
hard_trig_sx	initialize the FEE card in slot x for triggered readout
test_ad7417_sx	readout Voltage, currents and temperatures of FEE card in slot x (see 13.3.4)
set_hv_max_s4	set all bias Voltages to maximum (see 18.2)
set_hv_0_s4	set all bias Voltages to minimum (see 18.2)

Application developers and users are well advised to use only tested DCS scripts, however for full debugging and development the user may have to edit scripts or execute specific commands manually. The vi editor and scp copy command can be used on the DCS Linux system. There are direct commands, and delayed commands which are first stored in an instruction memory, terminated by a marker and then executed by an execute command. For delayed commands there are jump and loop instructions relative to an address of the 256 deep instruction memory at 0x7000.

Note: *If the strict time sequence of commands is important, like the readout of AD7417 registers after a 2 ms conversion command delay, a single delayed command sequence should be used with embedded RCU wait commands.*

The 40 bit GTL bus protocol corresponds in the DCS script language to two successive instructions of 20 bit (5 hex digits) hence there are two lines for a 40 bit write instruction, distinguished by a "position" bit. For read instructions, the upper 20 bit may be ignored, hence there is only 1 line of instruction for read operations. Finally there are bits which distinguish between broadcast and direct addressing, and a bit which selects one of the two RCU bus branches, namely A or B.

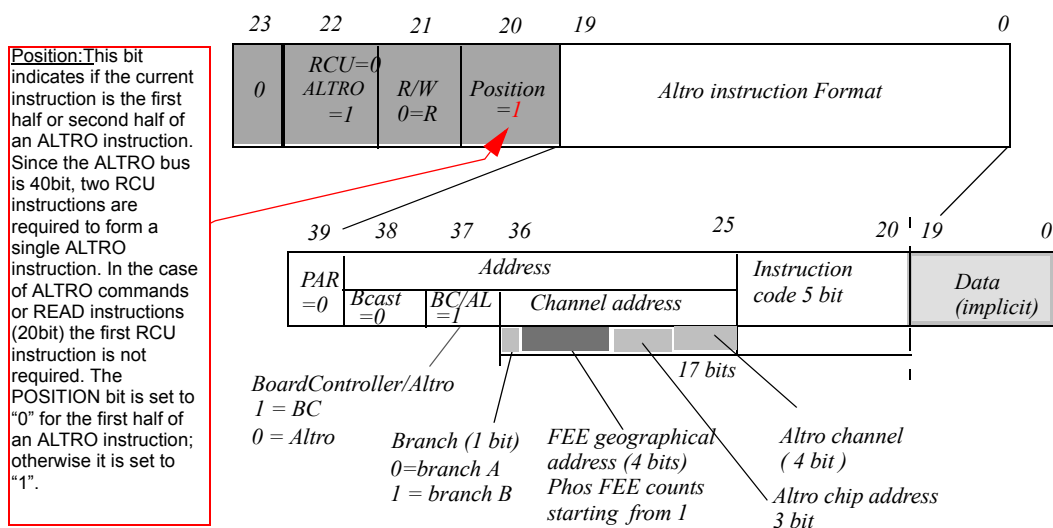
The formats of the DCS write and read instructions are decoded in Figure 219 Figure 220 below .

30.1 Delayed read/ write instructions

The communication with ALTRO and board controller is (apart from global registers) based on instructions which are first loaded in an instruction memory and then executed. The details of the codes to be stored in the instruction memory are shown in Figure 219 and Figure 220. The 12 bit channel address of the Altro is here composed of 3 fields (FEE address, Altro address, Altro-internal address) of which depending on the address mode and properties of the individual registers, some fields can be redundant. For example in a broadcast write to an Altro configuration register, only the FEE card field is required. In case of reading registers which belong to a channel, like the VFPED auto-calibration value, all 3 fields are required.

Figure 219 below shows the DCS decoding for a single line 20 bit read instruction.

Figure 219 decoding of delayed Altro-type READ instruction (0x5xxxxx)



Example for delayed read instruction: Store in the instruction memory (0x7000) a read instruction for bias control register at offset 0x41 on FEE card address 3 on branch B

w 0x7000 0x533041

If the FEE card is on Branch A and located at address 4:

w 0x7000 0x524041

The instruction memory (24bit x 256) at base address 0x7000 is loaded with a read instruction to be executed later by the execute instruction (Figure 219) . The instruction 0x523041 is decoded as follows (bit 23 always =0)

bit 23,22,21,20= 0101b= 0x5 Altro read instruction, position 1

bit 19,18,17,16= 0011b= 0x3 normal instruction, branch B

(for branch A this would be: 0010b= 0x2)

bit 15,14,13,12= 0100b= 0x3 FEE card in geographical position 3 (PHOS starts at 1)

bit 11,10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0 = 0000 0100 0001 = 0x041 Register address

The end -of-script instruction is placed in the memory:

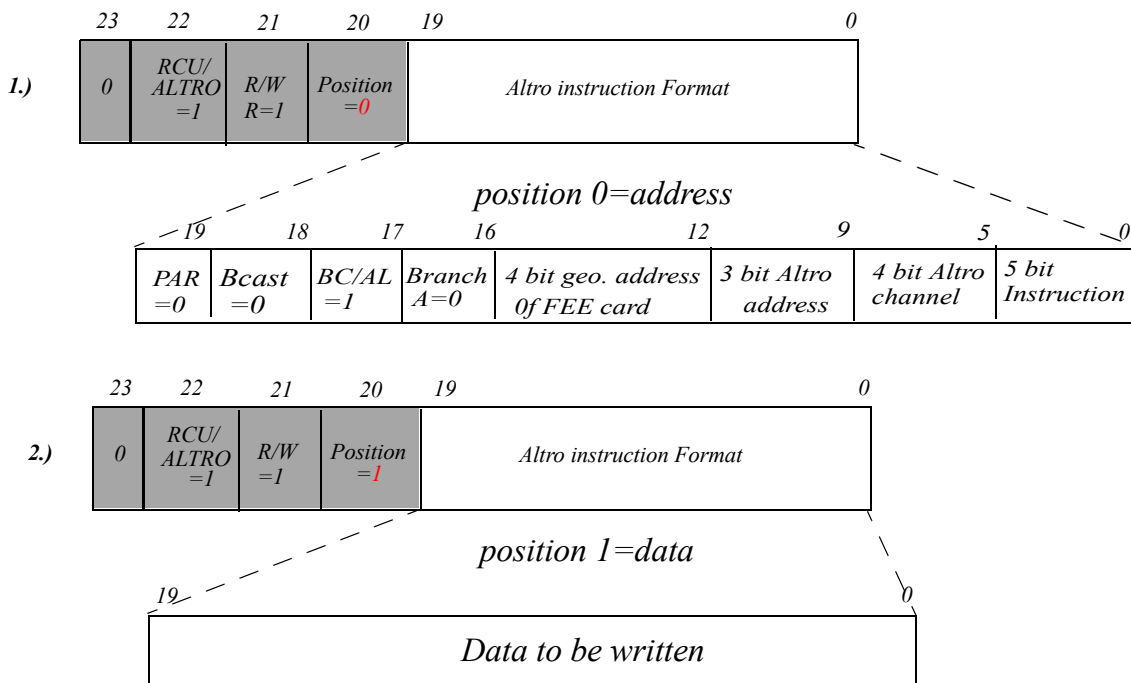
w 0x7001 0x390000

Exeecute the instruction memory starting from offset 0x0

w 0x0 0x0 .

Example: for a delayed write instruction to register address 0x40 on FEE card address 3 and branch A.

Figure 220 decoding of buffered 40 bit Altro WRITE instruction: 2 DCS lines 0x6xxxxx + 0x7xxxxx



Due to the 40 bit Altro bus, writing requires two 20 bit instructions, first 20 bit address, then 20 bit data

w 0x7000 0x623040 # part 1 (address) of 40 bit write instruction to register 40. branch A, address 3

w 0x7001 0x70029A # part 2 (data=0x29) of 40 bit write instruction

the instruction memory at base address 0x7000 and 0x7001 is loaded with a write instruction to be executed later (w 0x0 0x0) (Figure 220). The instruction 0x623040 is decoded below as follows (bit 23 always =0)

bit 23,22,21,20= 0110b= 0x6 1-st part of 40 bit Altro write instruction, position 0

bit 19,18,17,16 = 0x2 address is on branch A

bit 15,14,13,12 = 0x3 geographical address of FEE card is 3

bit 11,10,9,8,7,6,5,4,3,2,1,0 = 0x040 (12 bit register address)

The second part of the instruction 0x70029A is decoded as

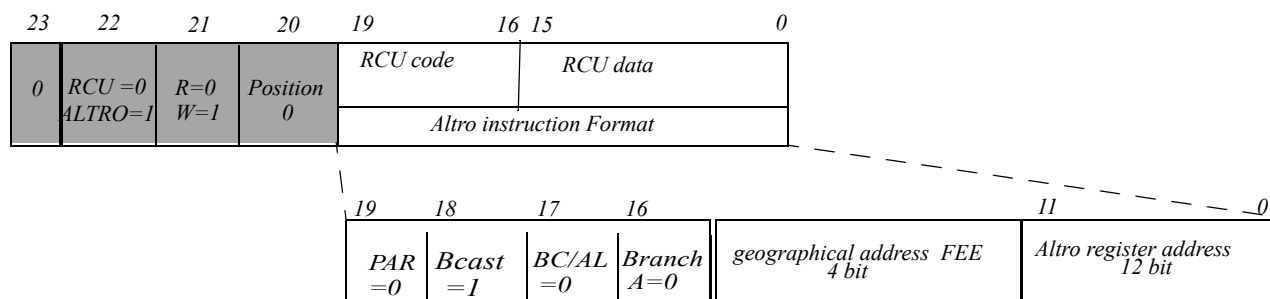
bit 23,22,21,20= 0111b= 0x7 2nd part of 40 bit Altro write instruction, position 1

bits 19....0 = 0x0029A is the value written to the previously defined register

30.2 Direct ALTRO write instructions

Broadcast instructions can be directed to all Altro registers of an FEE card, they are decoded as 24-bit instructions according the format

:

**Figure 221** Decoding of direct RCU/Altro broadcast instruction

Examples of 24 bit (6 digit) directed write operations:

- 1.) w 0x64000a 0xA9 # broadcast command to Altro Trigger Config Register 0x0A
---> 0x125 =295 samples from L0 trigger to end of acquisition
- 2.) w 0x64000c 0xf # broadcast command to all Altro Data path configuration register DPCF2
4 MEB buffers and 15 pre-samples

The Altro registers and commands are shown in Table 14 below

Table 14 Altro registers (selection for PHOS, for complete information, see [3])

Register Name	Address	Data fields (20 bit)	Comments
Altro trigger configuration	0x0A	<9:0> ACQ_END <19:10> ACQ_START	ACQ_START : number of cycles to wait before acquisition starts. Must be less or equal than ACQ_END = number of cycles elapsed from trigger to acquisition end. When Pre-trigger is used (see 0x0C), then ACQ_START is ignored.
Data path configuration 1	0x0B	<4:0> BC1_CFG <11:5> BC2_CFG <19:12> ZS_CFG	Default all 0 bit 19 enables zero suppression
Data path configuration 2	0x0C	<3:0> PTRG <4> NBUF <5> FLT_EN <6> PWSV	PTRG Nr. of pre-triggers, max 0xF NBUF Nr. of MEB buffer 4 or 8 FLT_EN enable bit digital filter PWSV, power-save bit (see 30.11)
Pedestal Memory address	0x0D	<9:0> PMA	adres of pedestal memory to be read or written

Table 14 Altro registers (selection for PHOS, for complete information, see [3])

Register Name	Address	Data fields (20 bit)	Comments
Altro Error status register	0x10	<2:0> Read Pointer <5:3> Write Pointer <9:6> Remaining Buffers <10> FULL <11> EMPTY <12> Parity Error <13> Instruction Error <14> Trigger Overlap <14> MMU 1 SEU <15> MMU 2 SEU <17> INT 1 SEU <18> INT 2 SEU <19> RDO Error	
Chip Address and Event Length	0x11	< 7:0> EVL <15:8> HADD	EVL: Length (in 40-bit words) of the last event stored in the data memory HADD: Hard-wired Chip Address (fixed)
Trigger counter	0x12	<15:0> TRCNT	read only: Number of triggers received
Write pointer increment command	0x18	none	This command is equivalent to the Level 2 Trigger Accept.
Read Pointer Increment command	0x19	none	releases a buffer of the Data Memory, making it available for writing new data. Typically used after Channel readout.
Channel readout (macro) command	0x1A	none	This software trigger command comproduces the readout of the Altro channels specified in the active channels memory at 0x6400. This command should be issued after level -1 and level-2 triggres were sent. The readout starts immediately after the command is acknowledged. During the readout, the ALTRO becomes the owner of the bus. After the transfer, the memory buffer must be freed by the Read Pointer increment command.
Software trigger command	0x1B	none	sends a Level 1 trigger which is entirely equivalent to the L1 line,
Command: Clear Altro Trigger counter	0x1C	none	sets trigger counter to 0.
Command: Clear Altro Error register	0x1D	none	

30.3 RCU interface registers [24]

A subset of the global addresses for RCU control is shown in Table 15 .

Table 15 some RCU top level commands

Name	Access	Size	Base address	Description
FEC	R/W	32b	0x8000	Contains the active cards list. The lower 16 bit correspond to branch A, the upper 16 bit correspond to branch B. A bit is set to 1 if the card is active. RCU can remove cards from the active in case of hard interrupts;
RDOL	R/W	32b	0x8001	Corresponds to Active Card list but RCU can remove cards from the Readout List in case of soft interrupts; the card remains ON and is able to reply to commands
DCS_ON	W	1b	0xE000	Make DCS card master of the RCU bus
DLL_ON	W	1b	0xF000	Make DLL link master of RCU bus
L1_TTC	W	1b	0xE800	Enable L1 trigger from TTC
L1_CMD	W	1b	0xD800	Enable L1 trigger issued by Command (default)
L1	W	1b	0xD000	send L1 trigger if L1_CMD has been set
GLB_RESET	W	1b	0x2000	Reset both RCU and FEE cards
FEC_RESET	W	1b	0x2001	Reset only EE cards
RCU_RESET	W	1b	0x2002	Reset only RCU

Table 16 shows 8 registers of which two (ERRST and TRCFG) are frequently used in configuration scripts

Table 16 some status registers

Name	Access	Size	Base Address	Description
ERRST	R	32b	0x7800	contains status and error bits
TRCFG	R/W	32b	0x7801	contains trigger configuration and status

30.4 ERRST Error status register 0x7800

The error status register ERRST of Figure 222 is read at address 0x7800 and is to be read back as zero.

r 0x7800 # read ERRST should be zero

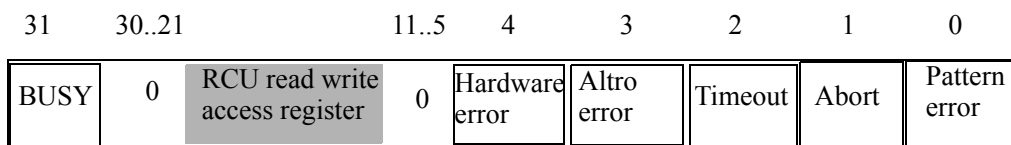


Figure 222 Error status register ERRST (details see [24] RCU firmware manual)

Note: In case of an error condition “Altro Error” the error line on the Altro bus is set and there are no more ACK acknowledgements, hence the register must be cleared via the instruction.

w 0x6c01 0x0

Typical error readbacks are:

0x0004 = timeout, the FEE card did not reply in 32 clock cycles

0x0008 = Abort = error status on the GTL bus

0x0010 = Hardware error

Note: In case of such a non-zero readback status, the error must be found and corrected since all following instructions are not reliable

30.5 Altro Interface on RCU [24]

A subset of the commands for the Altro interface on the RCU is shown in Table 17

Table 17 Altro interface commands

NAME	Access	Base Address	Description
RS_STATUS	W	0x6C01	Resets the ERRST (status) register
RS_TRCFG	W	0x6C02	Resets the TRCFG (trigger configuration) register
RS_TRCNT	W	0c6C03	Resets the TRCNT (trigger counter)
EXEC	W	0x00xx	Starts execution from instruction memory at 8 bit offset xx
Abort	W	0x0800	Aborts execution of instruction memory sequence

30.6 Buffered instructions

Delayed Altro instruction are stored in a 256 deep instruction memory at 0x7000. If a line in the execution **Table 18** Altro buffers and memories

Name	Size	Base Address	Description
Instruction Memory	24bit x 256	0x7000	Instruction buffer
Pattern MEM	10bit x 1024	0x6800	Pedestal values
Result MEM	20bit x 128	0x6000	Result of each Altro read instruction corresponding the the instruction buffer
Active Channel List	16bit x 256	0x6400	List of all channels to be read out. Each line corresponds to 1 Altro, each bit to one channel
Data MEM 1-Low	20bit x 256	0x7400	Low 20 bit of Altro data Memory 1
Data MEM 1-High	20bit x 256	0x7500	High 20 bit of Altro data Memory 1

sequence is a read instruction, the result is stored in a corresponding result memory. The list of all Altro buffers is shown in Table 18

30.7 JUMP/WAIT instructions[24]

For list execution of the instruction memory, the JUMP (or Loop) and WAIT instructions as defined below.

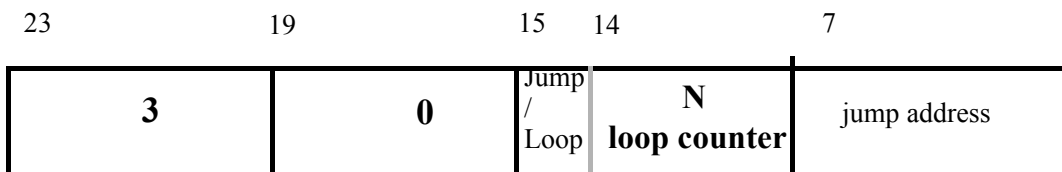


Figure 223 Jump / Loop instruction

Note: The RCU wait instruction is different from the DCS wait instruction. The latter generates a software “sleep”

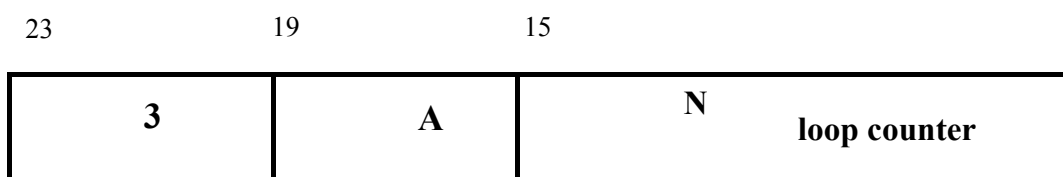


Figure 224 Wait instruction (N = number of readout clock cycles)

which is not strictly time synchronous with the other DCS commands.

30.8 FEE card initialization for triggered readout

The FEE card readout via the RCU is initialized via user-specific scripts to be executed on the DCS card.

There are numerous options for Altro-based readout via the RCU.

The initialization scripts define globally:

- Readout list, i.e. address of FEE cards and number of channels per FEE card (Chapt 31.1)
- trigger mode, i.e. external trigger or software trigger (TRCFG chapt 30.9)
- Altro ADC: samples, pre-samples, Number of buffers (DPHCF2 30.11)
- If required, Altro processing modes: zero-suppression, pedestals

30.9 TRCFG =RCU Trigger Configuration and Multi-Event Buffer Status register at address 0x7801

The TRCFG register must be correctly defined before the data readout. It defines the trigger mode (external, or software) and the partitioning of the Altro-internal Multi-Event Buffer

Table 19 TRCFG register

WRPT<31:29>	RDPT<28:26>	FULL	EMPTY	REMB<23:20>	X	POP	OPT	MODE<16:15>	BMD	TW<13:0>
-------------	-------------	------	-------	-------------	---	-----	-----	-------------	-----	----------

Table 20

Parameter	Description	Range
TW	Trigger mode 2: This register contains the number of clock cycles that the system waits after arrival of the L1 trigger before issuing the L2 trigger	0-3FFF
BMD	Buffer Mode: " 0 " for 4 buffers and "1" for 8 buffers	0 - 1
MODE	Trigger Mode: 0 Software trigger (default) 2 External L1 trigger and auto-generation of L2 after Nr of clocks defined by TW 3 External L1 and L2 trigger	0 - 3
OPT	This bit enables the readout optimization using the PCM	0 - 1
POP	This bit enables the popped readout scheme controlled by an external master e.g. USB or DCS	0 - 1
REMB	Remaining free buffers in the Multi event buffer	0 - F
EMPTY	Signals that the Multi-Event Buffer has no signals to read out	0 - 1
FULL	Signals that the Multi-Event Buffer is full and cannot accept new events	0 - 1
RDPT	Read Pointer position for MEB	0 - 8
WRPT	Write pointer position for MEB	0 - 8

30.10 TRCFG =ALTRO Trigger configuration register 0x0A

Altro-resident CRFG registers define the samples stored in the MEB relative to the L0 trigger

Table 21 TRCFG register 0x0A

<19..10>	ACQ-START	<9..0>	ACQ-END
----------	-----------	--------	---------

- ACQ_START number of cycles to wait before acquisition of samples starts. Must be less or equal than ACQ_END = number of cycles elapsed from trigger to acquisition end. When Pretrigger is used (see DPHCF2 register at 0x0C), then ACQ_START is ignored

30.11 DPHCF2 Data path configuration / pre-trigger Altro register 0x0C

There are two data path configuration registers in the Altro chips, of which DPHCF2 is important for the initialization of Pre-trigger and the partitioning of the data buffer in 4 or 8 buffers.

Table 22 DPHCF2 register 0x0C

dont care <19:7>	PWSW<6>	FLT_EN <5>	NBUF <4>	PTRG<3:0>
---------------------	---------	------------	----------	-----------

- PTRG number of pre-samples (max 15)
- NBUF 4 or 8 data memory buffers
- FLT_EN Enable digital filter
- PWSV Power save outside of trigger windows

31 Triggered readout

Event buffering in the Multi Event Buffer (MEB) of the Altro chips is conditioned by two strictly sequential timing signals, L1 and L2, which open and close the event sample recording, i.e. the L1 signal starts recording of Altro ADC samples and the L2 confirms (closes) the buffer. There are optionally 4 or 8 buffers in the MEB. After L2, the RCU issues a CHRDO readout macro which passes sequentially mastership to each individual Altro, which transfer the requested Number of channel data to the RCU. Hence events are received by the RCU in blocks which are fragmented per Altro chip.

The external trigger mode 2 generates L1 on reception of an external trigger and generates an internal L2 strobe after a number TW of clock cycles (TW parameter is part of the initialization).

The software trigger mode 1 generates both L1 and L2 via a software loop in the DCS scripts.

The trigger mode used in this document is the external L1 trigger, provided from the pulser to the RCU. :

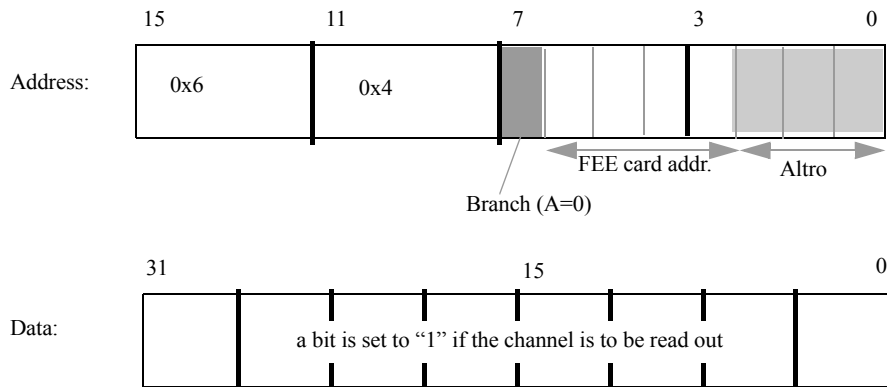


Figure 225 Coding of readout command for active channel list (ACL)

31.1 Altro channel Readout List

The definition of the Altro channel readout list for the PHOS CHRDO channel readout is based on the fact that the 4 Altro chips on the PHOS FEE cards are coded at address 0,2,3,4

Note: on the PHOS FEE, Altro address #1 is NOT existing

The coding is as shown in Figure 225

Example:

w 0x6400 256 0x0000	# clear active channel list
w 0x6498 0xffff	# all channels on Altro addr. 0, Branch B, geo address 3
w 0x649A 0xffff	# all channels on Altro addr 2, Branch B, geo address 3
w 0x649B 0xffff	# all channels on Altro addr 3, Branch B, geo address 3
w 0x649C 0xffff	# all channels on Altro addr 4, Branch B, geo address 3

31.2 Software trigger

The software trigger replaces the externally triggered Readout Command Macro by a software-generated Channel readout command CHRDO (address 0x1A see Table 14).

The CHRDO macro gives bus mastership to those Altro channels whose Active Channel and Readout List is set to "1". The Active Channel List list is to be written to base address 0x6400 using the format of Figure 225.

This CHRDO command must only be issued after level -1 and level-2 triggers were sent. The readout starts immediately after the command is acknowledged: The Altro's take bus mastership in sequence of the list stored in issuing the TRSF signal (see Figure 210 and Figure 212.) After the transfer, the Altro memory buffer must be reset by the Read Pointer increment command.

Appendix

1. FEE card transport and packaging

It is very important to transport FEE cards in antistatic material¹. Static charge can otherwise destroy optocouplers, shaper amplifiers, voltage regulators. Even the HV protection diodes specified up to 1.500 Volt have been found destroyed in non-adequate transport material.

2. Example script for readout of T,V,I from the three AD7417 chips

1. this is not a precaution advice, FEE cards will get damaged when transported in standard plastic bags.

```

enter operation (h/i/q/r/w):b s_pcmtva      # Read the data from AD7417 by sending STCNV command
                                           # author FeiFei Zou, HUST

executing: w 0x8000 0x00000010             # enable FEE card address 4 branch A

executing: wait 1 s

                                           # load execution memory at 0x7000

executing: w 0x7000 0x62401b               # sending 00 to address 1b = start conversion ( 0x1d in old PCM)

executing: w 0x7001 0x700000               # in PCM version > 2.0 conversion is automatic !

executing: w 0x7002 0x390000

                                           # RCU wait instruction to wait for conversion
executing: w 0x7003 0x3affff               # RCU wait instruction
executing: w 0x7004 0x3affff

                                           # start conversion command at 0x7000
executing: w 0x0 0x0                       # read error register
executing: r 0x7800
0x7800: 0

                                           # read data TEMP1= temperature IC13 ( Register 0x6)
executing: w 0x7000 0x524006               # read data D4V2 =Digital 4.2 Voltage (Register 0x7)
executing: w 0x7001 0x524007               # read data D4V2C=Digital Current 4.0V (Register 0x8)
executing: w 0x7002 0x524008               # read data D3V3 =Digital 3.3 Voltage (Register 0x9)
executing: w 0x7003 0x524009               # read data D3V3C =Digital Current 3.3V (Register 0xA)
executing: w 0x7004 0x52400a
executing: w 0x7005 0x390000
executing: wait 1 us
executing: w 0x0 0x0
executing: wait 1 us
executing: r 0x7800
0x7800: 0

                                           # load execution memory at 0x7000
executing: r 0x6000 5
0x6000: 0x78 0x1ed 0x4 0x1f7 0x06         # Temp1, d4v2, d4v2c, d3v3, d3v3c

```

RESULTS

TEMP1 IC13 = 0x78 /4 = 30 C

Voltage D4V2 = 0x1ed * 2.441 mV / 0.3037= 3.96 Volt (nominal= 4.2V)

Current D4V2C = 0x4 * 2.441 mV/0.27 Ohm /0.3037= 0.119 A (nominal =0.14A)

Voltage D3V3 =0x1f7 * 2.441 mV / 0.379= 3.32 Volt (nominal=3.3 V)

Current D3V3C= 0x06 * 2.441 mV/0.15 Ohm /0.379= 0.25A (nominal =0.31A)

continued next page...

executing: wait 1 us

```

executing: w 0x7000 0x524028      # load instruction memory at 0x7000
executing: w 0x7001 0x524029      # read data TEMP2= temperature IC 14 ( 0x28)
executing: w 0x7002 0x52402a      # read data A4V0 = 4V analog Voltage ( 0x29)
executing: w 0x7003 0x52402b      # read data A4V0C = 4V analog current ( 0x2A)
executing: w 0x7004 0x52402c      # read data A13V0 = +13V analog Voltage ( 0x2B)
executing: w 0x7005 0x390000      # read data A13V0C = +13V analog Curent ( 0x2C)
executing: wait 1 us
executing: w 0x0 0x0
executing: wait 1 us
executing: r 0x7800
0x7800: 0
executing: r 0x6000 5
0x6000: 0x7d 0x218 0x9 0x1ee      # Temp2, a4v0, a4v0c , a13v5, a13v5c
0x6004: 0x01

```

RESULTS

TEMP2 IC14 = 0x7d / 4= 31.2 C

Voltage A4V0 = 0x218 * 2.441mV / 0.379 = 3.4 V (nominal =4 V)

Current A4V0C = 0x9 * 2.441 mV / 0.15 OHm / 0.379 = 0.386A (nominal =0.34A)

Voltage A130V = 0x1ee * 2.441mv / 0.091 = 13.2 V (nominal =13 V)

Current A13V0C = 0x01 * 2.441mV / 1.2 / 0.091 = 0.02 A (nominal = 0.14 A)

Remark: current A13V0C measures current of external preamplifier !

```

executing: w 0x7000 0x524038      #read data TEMP3 = temperature IC15 ( 0x38)
executing: w 0x7001 0x524039      #read data AM6V0 analog Voltage -6V ( 0x39)
executing: w 0x7002 0x52403a      #read data AM6V0C current analog -6V ( 0x3A)
executing: w 0x7003 0x52403b      # read data A6V0 , +6 Volt analog (0x3B)
executing: w 0x7004 0x52403c      # read data A6VC , current +6V analog (0x3C)
executing: w 0x7005 0x390000
executing: wait 1 us
executing: w 0x0 0x0
executing: wait 1 us
executing: r 0x7800
0x7800: 0
executing: r 0x6000 5
0x6000: 0x78 0x132 0x0 0x1f7      # temp3, am6v0, am6v0c, a6v0, a6v0c
0x6004: 0x7

```

RESULTS**# TEMP3 IC15 = 0x78 /4 = 30 C****# Voltage AM6V0 = 0x13c * 2.441 mV / 0.5 -8.2V = -6.6 V (nominal -6V)****# Current 4M6V0C = 0x00 * 2.441mV /0.379 /0.22 = 0.0 A (nominal 0.32)****# Remark: current 4M6V0C measures current of external preamplifier !****# Voltage A6V0= 0x1f7 * 2.441 mV / 0.213 = 5.82 V (nominal +6V)****# Current A6V0C = 0x07 * 2.441 / 0.213 / 0.33 = 0.24A (nominal 0.32)**

3. Script for external trigger initialization (mode 2)

```

w 0x8000 0x00000010          # switch on FEE cards 4 on Branch A

wait 10 us

w 0x8001 0x00000010          # Define readout list: FEE card 4 on Branch A

wait 10 us                    # if successful, LED's on selected FEE card(s) are blinking

# .....set up of readout channels ACL list.....do not enable Altros channels which are not in
# the active frontend card list ....

w 0x6400 256 0x0000          # clear Active Channel List in memory

wait 10 us                    # Now select all Altros and their readout channels:

.....only as comment.....    # activate Altros at brach A, FEC 2

                                #w 0x6410 0xffff
                                #w 0x6412 0xffff
                                #w 0x6413 0xffff
                                #w 0x6414 0xffff

.....only as comment.....    # activate altros at branch A, FEC 3

                                #w 0x6418 0xffff
                                #w 0x641a 0xffff
                                #w 0x641b 0xffff
                                #w 0x641c 0xffff

.....#active Altros at branch A, FEC 4

w 0x6420 0xffff              #all channels on Altro address 0, Branch A, slot 4

w 0x6421 0xffff              #all channels on Altro addr. 1, branch A, slot 4 ( ! not existing)

w 0x6422 0xffff              #all channels on Altro address 2, Branch A, slot 4

w 0x6423 0xffff              #all channels on Altro address 3, Branch A, slot 4

w 0x6424 0xffff              #all channels on altro address 4, Branch A, slot 4

```

Figure 226 DCS script for initializing triggered readout for slot x=4 (hard_trig_s4.scr)

...continued from previous page

.....Trigger mode 2 (ext.)..... Note: during initialization all triggers must be disabled

.....first set up active frontend card list AFL. do not enable FEE cards which are not in the ACL readout channel list!(timeout)

.....set up Altro sampling mode set up instuction memory: Configure Altro for readout

```

w 0x7000 0x64000a      # broadcast command to Altro Trigger Config Register 0x0A

w 0x7001 0x7000A9      # ---> 0x125 =295 samples from L0 trigger to end

                        #....add some presamples for total No. of samples

w 0x7002 0x64000b      # broadcast command to Altro Data path config register DPCFB

w 0x7003 0x700000      # ---> set default

w 0x7004 0x64000c      # broadcast command to Altro Data path config register DPCF2

w 0x7005 0x70000f      # set number of MEB buffers to 4 and use 15 pre-samples

w 0x7006 0x390000      # close instruction memory

wait 1 us

w 0x7801 0x10bb8        # set TRCFG trigger config. register Trigger Mode =2,

                        # four buffers for the Altro MEB

                        # Tw= 0xbb8 = 3000/4 clocks between L1 and L2 = 78 us

                        # for 40 MHz readout clock

w 0xf800 0x1            # enable mezzanine card trigger on S2

                        # for TTC trigger use address 0xE800

                        # now external L0 triggers can be received and

                        # L2/CHRDO readout starts

w 0xf800 0x0

w 0x0 0x0

r 0x7800

```

4. Component References for a full test systemT

Table 23 Component referenecs for FEE test laboratory

Component	Technical reference	CERN SCEM / Pool	Other
TTi Pulse Generator	tpg 110		up to 10 V, 50 ns square
signal cables 50 OHM		CERN 04.69.11.065.x	user defined length
APD/CSP	APD: Hamamatsu S8148 CSP: Made in Japan GEFR GN-0261-3 6-wire Molex cable with 1.25 mm connector 51021-0600		1 CSP [14] 1 APD PHOS Project, [13] Toru Sgitate, Hiroshima University, contacts: -sugitate@hiroshima-u.ac.jp -iouri.sibirak@cern.ch
LED Flasher	see chapter 25.1 LEDs: Kingbright L-7104PBC		CERN PCB under development
T-card	Phos 8-channel Tcard May 2005, Made in Japan Reference 1GEFR GN-0535-1 Phos 16-channel T cards, July 2007		PHOS Project, [13] Toru Sgitate, Hiroshima University, contact: sugitate@hiroshima-u.ac.jp
IPCB with flat cable and connectors	Cable: 40 wire IDC cable 1.27 mm 1.) Mates with T-card: 40 pin Crimp connector: 3M connector (3940-2000 T) 2.) Crimp cable to IPCB: Spoerle 7840-0000 PR 40 pol / 2 REIHIGER/ PL-STV 3.) Mates with FEE Connector: Samtec LS2-130-01SD	IDC-D-Sub 3M Cable connector, CERN SCEM 09.21.20.130.9	IPCB: Production Capinor Norway, contact B.Skaali@fys.uio.no
Fast or cable for Trigger output to TRU	Samtec FFSD-08-D-20 16 pin, 1.27 mm		length 40 cm
Altera Byteblaster Jtag adapter for programming FEE	EBV PLBYTEBLASTER-II		www.altera.com
Xilinx parallel cable IV	XLXHW-PC4	DAI 1855992	www.xilinx.com
FEE card	CERN No. 0000042476 V1.1a	EDMS under Alice Engineering Baseline / PHOS Spectrometer/Alice PHOS FEE	Production via HUST Wuhan, P.R. China, contact: D. Zhou, email: zdc@iopp.ccnu.edu.cn PHOS project, CERN/HUST [6][4]
GTL bus strips	EDA-00711-V1 Data EDA-00712-V1 Ctrl corrected versions for cable connection to RCU [4] Cables: 2 mm centerline IDC assembly Data cable: 2 mm Samtec TCMD-25-T-15.00-01 Control cable: Samtec TCMD-20-T-15.00-01 Data bus connectors: 54 pin MMS-127-01-L-DV Control bus connectors: 30 pin SAMTEC MMS-115-01-L-DV		See chapter 12 PCB produced by Capinor Norway, contact B.Skaali B.Skaali@fys.uio.no Component (resistors, capacitors, cable) mounting Cables: On GTL side, male connectors. On RCU-side cable, female crimp connectors
LV Power Supplies FEE test in laboratory only		<u>Only for Laboratory single FEE card test:</u> Gossen Konstanter LSP	25V/1A, 25V/1A, 7V/5A
LV Power Supplies for Experiment	1.) Wiener OM11.0001 5 channels of 6 used for 1 PHOS module 2.) Wiener OM11.0004 1 channel of 12 used for 1 PHOS module	Water -cooled. Only for Experimental hall full module test. USB, Canbus and and Ethernet control	1.) 12* 5..15 V (22A) 2.) 6 * 2..8 V (115 A)

Table 23 Component referencs for FEE test laboratory

Component	Technical reference	CERN SCEM / Pool	Other
LV cables FEE	LV connector Phoenix MSTB 2, 5/ 8-GF-5, 08: 8-way power connector with 4 analog and 2 digital supply voltages	1.5 m cable 2.5 mm CERN 04.66.61.310.5	8 LV cables 2.5mm2 with either FASTON 6.3 mm or banana plug ends
HV Power Supply (test)		Oltronix B605 DS	or other +400 V, 10 mA
HV Power Supply Experiment	ISEG EHQ 8605p_156-F		8 * +500 V differential 15 mA
HV cable FEE	Connector FEE side: Lemo rated 500 V FFS.00.250.NTCE24 Connector HV side: Banana plugs	Lemo: CERN 04.61.11.90	50 OHM cable on FEE side, on HV supply sid: connect middle pin to + 400 Volt and shield to GND
HV daisy chain cable	coax cable 20 cm with crimped size 00 lemo connectors	CERN 04.69.11.065.6	any other cable length applicable as well
LV Power Supplies RCU	may be connected to FEE power supply 4.2 and 3.3V	Gossen Konstanter LSP	25V/1A, 25V/1A, 7V/5A required: 4.3 V 1.6 A and 3.3V 100mA
LV cables for RCU	Cable connector: Weidmuller BLZ 5.08/4 (Radiospares)		4 cables max 2.5 mm2 with banana connector ends
RCU-4	TPC project http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc/rcu.htm		contact: L.Musa @cern
RCU power connector	Weidmuller BL5.08/4	Radiospares 403-897	
DCS Linux card	KIP DCS board Vers 1.52 TPC configuration KIP Heidelberg, http://www.kip.uni-heidelberg.de/ti/DCS-Board/current/)		serial No maps to MAC address DCS card accessories -power cable, -Jtag adapter cable -Cat5e network cable -Serial line adapter Note: magnetics-free ethernet: MUST be connected to Ethernet Hub
SIU card Source Interface Unit V2.3			delivered by CERN DAQ project. To be used with dual optical fiber contact: Pierre.Vande.Vyvre@cern.ch
DDL fiber			dual fiber, multimode 50/125 um with LC connector on both sides. available by CERN DAQ project, contact: Pierre.Vande.Vyvre@cern.ch
TTC fiber			single mode optical fiber with ST connector
DRORC 64 bit PCI card			DDL PCI card, available by CERN DAQ project Pierre.Vande.Vyvre@cern.ch
L0-trigger adapter card			NIM-> LVTTTL Option for RCU if TTC trigger is not installed or available. see this document
Ethernet hub for DCS card (obligatory)	5 port N-way switch/hub 10/100 Mbps NSW-7005 or equivalent		For specifics, contact ti@kip.uni-heidelberg.de KIP Heidelberg
DAQ computer			Server PC, Scientific Linux, PCI-64, large HD CERN DAQ project Pierre.Vande.Vyvre@cern.ch

Table 23 Component referenecs for FEE test laboratory

Component	Technical reference	CERN SCEM / Pool	Other
Software on DAQ			Date-5 (DAQ project) Root-5 (CERN)
Firmware programmingsoftware on user laptop	www.altera.com www.xilinx.com	At CERN available for registered NICE users under: \\dsy-srv4\caeprgs\	Altera: - Quartus Programmer - exc_flash-programmer.exe Xilinx: -Xilinx ISE 7.1i Accessories: IMPACT
Firmware RCU-4	xxx.bit		from TCP WEB page http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc/firmware.htm Contact: Gonzalez.Gutierrez@cern.ch
PCM Firmware FEE	xxx.pof xxx.sof		PCM from HUST group Wuhan: contact qingxia_li@hust.edu.cn latest version: PCM 1.2
Firmware DCS	xxx.hex		TPC version for PHOS: special for each serial Number. Contact: johan.alme@ift.uib.no

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