CERN –PH/ED

RCU Firmware:

Registers & Commands

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Created: July 2004

Last Update: 18th December 2006

DRAFT 0.1

Chapter 1

Top Level Unit

1.1 Functionality

The data/configuration transfer between the RCU and front-end cards is performed with the ALTRO protocol as described in the ALTRO Chip User's Manual. From the User's point of view the ALTROs are not directly accessible from the RCU. The link is made through a μcontroller-like procedure that will execute sequentially a set of pre-loaded instructions. In this way the User can send large portions of front-end configuration in an instruction memory in the RCU and execute the sequence with a single command. These sequences can be composed with ALTRO instructions and RCU-specific instructions.

This manual contains full information on all accessible registers and memories as well as the macro instructions that can by run in the RCU. At the end of this document, some basic examples of configuration scripts (containing instruction sequences) are proposed. They allow running the system with a minimal set of parameters. The manual reflects the current version of the firmware and its functionality.

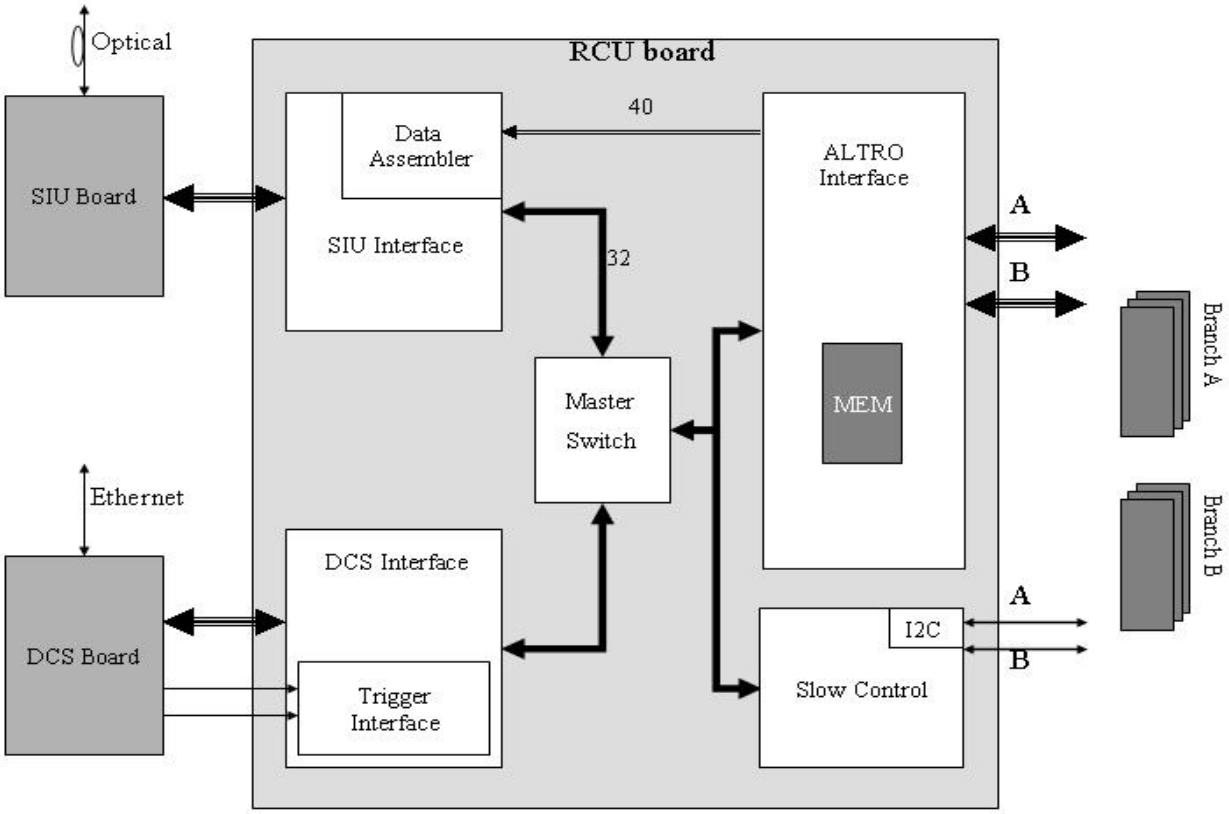

Figure 1.1: Block Diagram of TOP Module of the RCU Firmware

1.2 Global Registers and Commands

The global registers and commands for the overall RCU firmware that are briefly described in table 1.1. The register address is also given, however in the case of memories; it corresponds to the start address.

Global Storage and Command Table

Name	Access	Size	Base Address	Description
AFL	R/W	32bit	0x8000	This register, updated by the Slow Control contains the active front-end card list. The low 16bit correspond to branch A, whereas the higher 16bit correspond to branch B. A bit is set to “1” if a FEC is ON.
RDOL	R/W	32bit	0x8001	
DCSadd	16bit	16bit	0x8007	DCS address field stored in each write transaction
RCU_version	R/W	24bit	0x8008	RCU firmware version
Backplane_version	R/W	1bit	0x8009	TPC (0) or PHOS (1) version for the backplane
TTCclk_freq	R	3bit	0x800A	Frequency of the TTC clk
DCS_ON	W	1bit	0xE000	By executing this command, the DCS card becomes master of the RCU bus. (DCS access only)
DDL_ON	W	1bit	0xF000	By executing this command, the DDL becomes master of the RCU bus. Default condition. (DCS access only)
L1_TTC	W	1bit	0xE800	Enables the L1 trigger coming from the TTC chip
SCLKsync	W	1bit	0x8020	Re-synchronize the SCLK with the next L1TTC trigger
L1_aux	W	1bit	0xF800	Enables the L1 trigger coming from the dedicated connector
L1_CMD	W	1bit	0xD800	Enables the L1 trigger issued by a command (default)
L1	W	1bit	0xD000	Sends L1 trigger if L1_CMD has been previously set
GLB_RESET	W	1bit	0x2000	Resets both RCU and FECs.
FEC_RESET	W	1bit	0x2001	Resets only the FECs.
RCU_RESET	W	1bit	0x2002	Resets only the RCU. It does not affect to the AFL (0x8000) and Backplane_version (0x8009) registers
WRD_RD	W	1bit	0x5xxx	Number of words to be read (in DDL access only)

Table 1.1: Storage and Command Table

Chapter 2

ALTRO Interface Module

2.1 Functionality

The ALTRO Interface Module is responsible for the interface between the RCU and the front-end cards via the bidirectional 40bit bus and corresponding control signals.

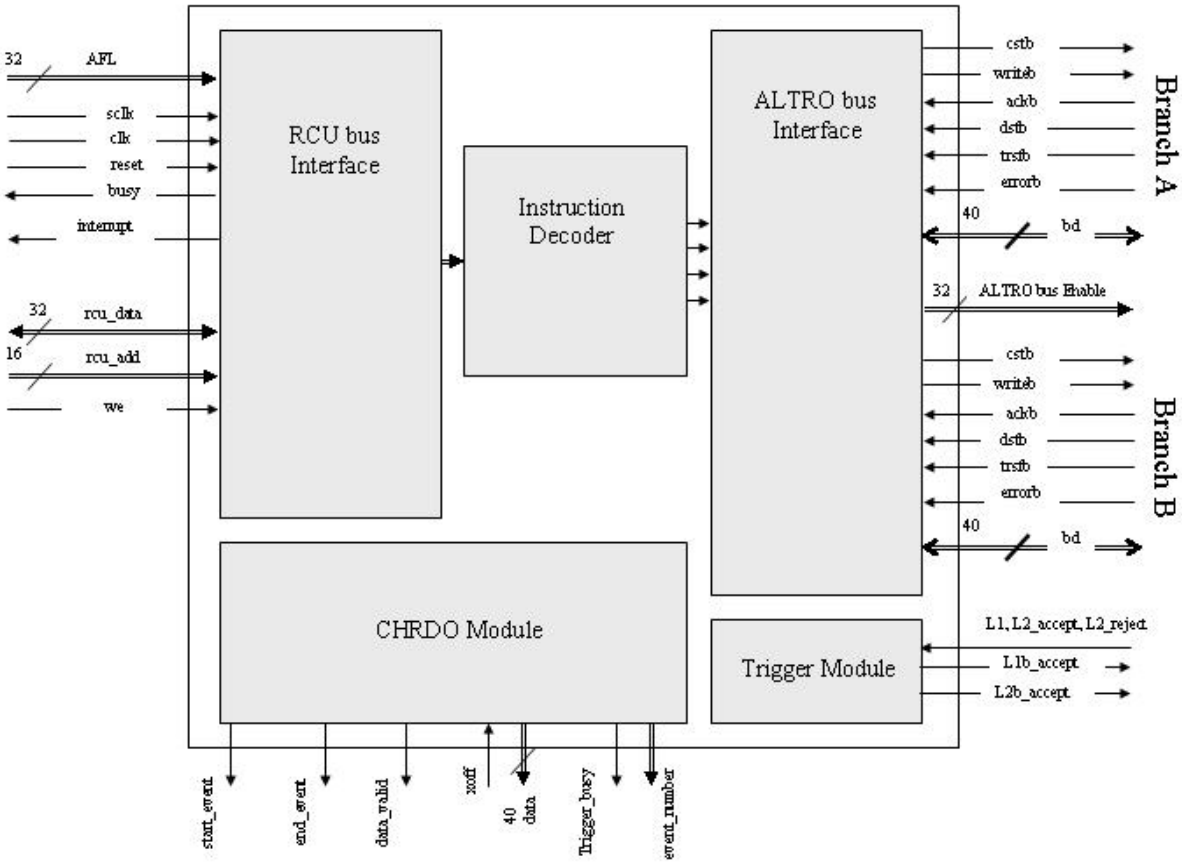

Figure 2.1: Block Diagram of the ALTRO Interface Module of the RCU Firmware

The most relevant ALTRO bus signals are summarized in table 2.1. A more detailed description of the bus signals is given hereafter.

ALTRO BUS				
Signal Name	Function	# bits	Dir.	Polarity
AD	Address / Data	40	Bi-directional	H
WRITE	Write / Read	1	Input	L
CSTB	Command Strobe	1	Input	L
ACKN	Acknowledge	1	Output	L
ERROR	Error	1	Output	L
TRSF	Transfer	1	Output	L
DSTB	Data Strobe	1	Output	L
LVL1	Level-1 Trigger	1	Input	L
LVL2	Level-2 Trigger	1	Input	L
GRST	Global Reset	1	Input	L
SCLK	Sampling Clock	1	Input	-
RCLK	Readout Clock	1	Input	-

Table 2.1 Signal summary.

AD[39:0] (bi-directional)

This is a 40-bit bi-directional Address/Data bus (table 2.2). It consists of three main fields that, starting from the least significant bit, are organised as follows: the *data* field (20 bits), the *instruction* field (5 bits) and the *address* field (14 bits). The most significant bit is a parity bit. It should be noted that, with a 14-bit *address* field, the ALTRO bus space sizes 16384. This addressable space is divided in two equal size partitions: the ALTRO chips partition (AL partition) and the Board Controller partition (BC partition).

39	38	37	36 29	28 25	24 20	19 0
PAR	**ADDRESS**				**INSTRUCTION CODE**	**DATA**
	BCAST	**BC/AL**	**CHANNEL ADDRESS**			

Table 2.2: 40-bit bi-directional Address/Data bus

AD[39] (PAR) is the parity bit of the 20 most significant bits. It is set such that the parity of the 20 most significant bits is always even. The parity bit allows the detection of a single bit error in the transmission between the RCU and the FEC.

When the bit AD[38] BCAST (broadcast) is set to 1, the *bus write cycle* initiated by the RCU (master) is addressed to an entire *partition* of the *address space* (AL or BC partition). In this case the slave units ignore the channel address field.

The bit AD[37] (BC/AL) defines the address space partition: 1 for the BC partition, 0 for the AL partition.

The following 8 bits AD[36:25] (CHANNEL ADDRESS) specify the *channel address* and, during an *instruction cycle*, are compared with the hard-wired address. From the most significant bit, the channel address consists of a branch address (1 bit), the FEC address (4 bits), the ALTRO chip address (3 bits) and the ALTRO's internal channel address (4 bits). This allocations of addresses is the recommended one and it corresponds to the case of a board containing 8 ALTROs (FEC) and an RCU with two branches each one with 16 FECs.

The bits AD[24-20] (INSTRUCTION CODE) carry the instruction code. As it will be detailed in the next section, the ALTRO chips and the BC are controlled by a set of instructions. The instruction can be either an access to a Configuration/Status Register (CSR), whose address is part of the instruction code, or a Command. In the former case, the instruction involves a WRITE or READ cycle, according to the value of the WRITE signal, to one of the CSRs. In the latter case the instruction does not imply a data transfer from/to the addressed unit, thus the data field of the AD bus is not used.

The data field AD[19-0] carries the data in the WRITE or READ instructions.

WRITE (Input)

The write/read signal is driven by the master (RCU) and defines whether the access to the addressed unit is in write/read mode (low/high).

CSTB (Input)

The master (RCU) drives the command strobe (CSTB) signal. When asserted, it indicates that a valid word has been placed in the AD bus. The signal also qualifies the WRITE signal. The master only releases the CSTB signal after the slave has asserted the ACKN signal. The only exception is represented by the *broadcast Instruction* cycles for which there is no acknowledge. In the latter case the master will keep the information on the bus and will validate it with the CSTB signal for at least 2 RCLK cycles.

ACKN, ACKN_EN (Output)

On a WRITE or COMMAND cycle, the addressed unit asserts the ACKN signal to indicate that is has successfully latched the bus content and executed the requested *instruction*. On a READ cycle, the addressed unit asserts the ACKN to indicate that it has placed the requested data on the bus. The only exception is represented by the broadcast instruction that does not have to be acknowledged. A signal ACKN_EN frames ACKN, enabling the intrinsic capacitor in the transceiver.

ERROR (Output)

The ERROR line is asserted by the slave units to signal the occurrence of an error condition. If the error condition has occurred in an instruction cycle (parity error or *instruction* code error), the slave does not acknowledge the instruction cycle and asserts the ERROR signal.

TRANSFER, TRANSFER_EN, DOLO_EN – DSTB (Output)

The readout of the ALTRO chip data memory is performed in two steps. The first one is a normal instruction cycle where the RCU issues the command with the instruction code CHRDO (channel readout). The ALTRO chip that, after a number of cycles, takes the control of the bus by asserting the TRANSFER signal acknowledges this instruction cycle. TRANSFER is kept asserted till the data block has been completely transferred. The data transfer is not necessarily continuous and for this reason each single word, being transferred, is validated by the signal DSTB (Data Strobe). TRANSFER_EN and DOLO_EN are used to drive the bi-directional bus AD when transferring an event, for the former and for reading a register for the later.

LVL1 – LVL2 (Input)

The LVL1 and LVL2 signals are broadcasted by the RCU to all the FECs. They are used for the distribution of the Level-1 and Level-2 trigger information. The LVL1 signal is synchronous with the SCLK signal and lasts for at least two clock cycles. The LVL2 signal is synchronous with the RCLK and lasts also for two clock cycles.

GRST – SCLK – RCLK (Input)

The GRST (Global Reset) is an active low global rest. It initialises all the internal registers, counters and state machines. The SCLK (Sampling Clock) is the ALTRO sampling clock and can have a maximum frequency of 20MHz. All the data ALTRO processing is done synchronously with the SCLK signal. The RCLK is the ALTRO readout clock and can have a maximum frequency of 40MHz. The latter is the clock engine for the ALTRO bus master and slave interfaces.

2.2 Size of Memories

There are 8 memory partitions in the ALTRO Interface Module that are addressable via the RCU bus in both READ and WRITE modes.

ALTRO Interface Addressable Memories

Name	Size	Base Address	Description
Instruction MEM	24bit x 256	0x7000	It contains the Instruction Sequence to be executed either in configuration or readout.
Pattern MEM	10bit x 1024	0x6800	Contains Pedestal values to be sent or compared.
Result MEM	20bit x 128	0x6000	The result of each ALTRO READ instruction is stored in this memory.
Active Channel List	16bit x 256	0x6400	It contains the list, in a per channel basis, of all the channels that will be readout. Each line corresponds to an ALTRO, and each bit to a channel.
Data MEM 1 - Low	20bit x 256	0x7400	Low 20bit of data MEM 1
Data MEM 1 - High	20bit x 256	0x7500	High 20bit of data MEM 1
Data MEM 2 - Low	20bit x 256	0x7C00	Low 20bit of data MEM 2
Data MEM 2 - High	20bit x 256	0x7D00	High 20bit of data MEM 2

Table 2.3: Addressable Memories on the ALTRO Interface Module

2.3 Register Table

The register Table, table 2.4, incorporates various registers that are used for configuration of the RCU or as status registers. A number of commands are also possible and are depicted in table 2.5. More details on those registers and commands are given subsequently.

ALTRO Interface Register Table

Name	Access	Size	Base Address	Description
ERRST	R	32bit	0x7800	It contains the status and error information.
TRCFG	R/W	32bit	0x7801	It contains the Trigger configuration and Trigger Status.
TRCNT	R	32bit	0x7802	It contains the counters of L1 triggers received and L1 triggers accepted.
LWADD	R	18bit	0x7803	It contains information used in popped readout mode.
IRADD	R	20bit	0x7804	It contains the address of the last instruction sent to the ALTROs.
IRDAT	R	20bit	0x7805	It contains the data of the last instruction sent to the ALTROs.
PMCFG	R/W	20bit	0x7806	It contains the configuration for the PMWRITE and PMREAD macros.
CHADD	R	24bit	0x7807	It contains the hardware address of the last channel being readout in both buffers.

Table 2.4: Register Table

ALTRO Interface Commands

Name	Access	Base Address	Description
RS_STATUS	W	0x6C01	It resets the ERRST (status) register
RS_TRCFG	W	0x6C02	It resets the TRCFG (trigger configuration) register
RS_TRCNT	W	0x6C03	It resets the TRCNT (trigger counter) register
RS_BUF1	W	0x6C04	Resets readout buffer 1. (In popped readout mode only)
RS_BUF2	W	0x6C05	Resets readout buffer 2. (In popped readout mode only)
EXEC	W	0x00**XX**	Starts the execution of a sequence in the instruction memory at the address specified in **XX** (8bits)
ABORT	W	0x0800	Aborts any sequence taking place on the instruction memory

Table 2.5: Command Table

ERRST

Error and Status register

Instruction Code	7800 h
Width	32
Register Type	Status
Access Type	Read/Write

Instruction Coding

31	30 21	20 12	11 5	4	3	2	1	0
BUSY	**0**	**RCU HWADD**	**0**	**HWADD ERROR**	**ALTRO ERROR**	**TIMEOUT**	**ABORT**	**PATTERN ERROR**

Write Access

Description

Parameter	Description	Range
PATTERN ERROR	This bit is set to “1” if there is a mismatch in the comparison of the PMREAD RCU instruction	0 – 1
ABORT	It signals that the instruction sequence has been aborted	0 – 1
TIMEOUT	This bit is set to “1” if the front-end cards do not respond within 32 clock cycles	0 -- 1
ALTRO ERROR	This bit corresponds to the errorb line of the ALTRO bus	0 -- 1
HWADD ERROR	This bits signals a mismatch between the channel address contained in the data of a readout and the channel address requested in that readout	0 -- 1
RCU HWADD	These 9 bits have both WRITE/READ access and encode the RCU hardware address: [2 0] – partition; [8 3] – sector.	0 – 1FF
BUSY	This bit indicates that the ALTRO Interface Module is busy and therefore the instruction memory is inaccessible.	0 - 1

TRCFG

Trigger Configuration and Buffer Status register

Instruction Code	7801 h
Width	32
Register Type	Config /Status
Access Type	Read / Write

Instruction Coding

31 29	28 26	25	24	23 20	19	18	17	16 15	14	13 0
WRPT	**RDPT**	**FULL**	**EMPTY**	**REMB**	**X**	**POP**	**OPT**	**MODE**	**BMD**	**TW**

Write Access

Description

Parameter	Description	Range
TW	This register contains the number of clock cycles that the system waits after the arrival of the L1 trigger and the issuing of the L2 trigger. Only usable in trigger mode = 2	0 – 3FFF
BMD	Buffer Mode: “0” for 4 buffers and “1” for 8 buffers	0 – 1
MODE	Trigger Mode: 0 Software trigger (default) 2 External L1 trigger and automatic generation of L2 after TW 3 External L1 trigger and external L2 trigger	0 -- 3
OPT	This bit enables the readout optimization using the board controller	0 – 1
POP	This bit enables a popped readout scheme controlled by an external master e.g. USB or DCS	0 – 1
REMB	Remaining free buffers in the multi-event buffer	0 -- F
EMPTY	Signals that the multi-event buffer has no events to be readout	0 – 1
FULL	Signals that the multi-event buffer is full and cannot accept any events	0 – 1
RDPT	Read pointer position	0 – 8
WRPT	Write pointer position	0 – 8

TRCNT

Trigger Counter

Instruction Code	7802 h
Width	32
Register Type	Status
Access Type	Read

Instruction Coding

31 … 16	15 … 0
Number of L1 triggers Received	**Number of L1 triggers Accepted**

Description

Parameter	Description	Range
NTR	Number of L1 triggers Received.	0 – FFFF
NTA	Number of L1 triggers Accepted	0 – FFFF

LWADD

Information needed for Popped Readout scheme.

Instruction Code	7803 h
Width	18
Register Type	Status
Access Type	Read

Instruction Coding

31 – 18	17	16	15 – 8	7 – 0
X	**BUFLAG2**	**BUFLAG1**	**LWADD2**	**LWADD1**

Description

Parameter	Description	Range
LWADD1	Address of last word written in buffer 1.	0 – FF
LWADD2	Address of last word written in buffer 1.	0 – FF
BUFLAG1	Flag indicating new channel readout in buffer 1.	0 - 1
BUFLAG2	Flag indicating new channel readout in buffer 2.	0 - 1

IRADD

Address of last ALTRO Instruction

Instruction Code	7804 h
Width	20
Register Type	Status
Access Type	Read

Instruction Coding

31 … 20	19 … 0
X	**Address of the last ALTRO instruction sent**

IRDTA

Data of last ALTRO Instruction

Instruction Code	7805 h
Width	20
Register Type	Status
Access Type	Read

Instruction Coding

31 … 20	19 … 0
X	**Data of the last ALTRO instruction sent**

PMCFG

Pedestal Memory Configuration

Instruction Code	7806 h
Width	20
Register Type	Configuration
Access Type	Read / Write

Instruction Coding

31 … 20	19 … 10	9 … 0
X	**End of block pointer**	**Begin of block pointer**

CHADD

Last channel address readout

Instruction Code	7807 h
Width	24
Register Type	Configuration
Access Type	Read

Instruction Coding

31 … 24	23 … 12	11 … 0
X	**Channel address stored in buffer 2**	**Channel address stored in buffer 1**

2.4 Instruction Sequence Code

The RCU instructions are coded in 24bit and can be divided into RCU-specific commands and ALTRO Instructions. In both cases the basic structure of each instruction is:

22	21	20	19 16	15 0
RCU/ ALTRO	**R/W**	**Position**	**RCU Instruction Code**	**RCU Instruction Data**
			ALTRO Instruction Format	

Table 2.6: 40-bit bi-directional Address/Data bus

1) **RCU/ALTRO**. It contains information on the type of instruction. This bit is set to “1” it is an ALTRO instruction and “0” for an RCU command.

2) **R/W**. This bit is set to “1” for a WRITE instruction or command and to “0” for READ access.

3) **Position**. This bit indicates if the current instruction is the first half or second half of an ALTRO instruction. Since the ALTRO bus is 40bit, two RCU instructions are required to form a single ALTRO instruction. In the case of ALTRO commands or READ instructions (20bit) the first RCU instruction is not required. The POSITION bit is set to “0” for the first half of an ALTRO instruction; otherwise it is set to “1”.

4) **RCU Instruction Code**. This 4bit register contains the code of the specific RCU command.

5) **RCU Instruction Data**. This 16bit register contains meaningful data related with specific RCU command. In some cases this field is not needed.

6) **ALTRO Instruction Format**. This 20bit field contains either the first or second part of an ALTRO instruction [ALTRO User’s Manual].

Table 2.7 shows a summary of the existing macro-instructions which are RCU specific. To note that on top of those, all the ALTRO commands and register accesses are possible. In this sense a given instruction sequence can contain a mix of ALTRO-specific commands and RCU macros. A more detailed explanation on each instruction is given subsequently.

Instruction Set: Summary Table

Name	Base Address	Description
JUMP	0x0	Jump or Loop Instruction.
RS_STATUS	0x1	This instruction sends a reset to the ERRST register.
RS_TRCFG	0x2	This instruction sends a reset to the TRCFG register.
RS_TRCNT	0x3	This instruction sends a reset to the TRCNT register.
CHRDO	0x6	This instruction sends the ALTRO CHRDO command to all the channels whose front-end card is active (cf. Active Front-end card List) and whose corresponding bit in the Active Channel List (ACL) is set to “1”.
PMREAD	0x7	This instruction sends the ALTRO PMADD (W) and PMDTA (R) commands to the channel with address CHANNEL ADDRESS and to all possible 1024 locations of the corresponding ALTRO pedestal memory. The result is compared with the content of the Pattern memory of the RCU. Any error in the comparison sets the bit[0] of the ERRST status register to “1”.
PMWRITE	0x8	This instruction sends the ALTRO PMADD (W) and PMDTA (W) commands to the channel with address CHANNEL ADDRESS to all 1024 locations of the corresponding ALTRO pedestal memory. The instruction is broadcasted to all channels if the bcast bit is set to “1”.
END	0x9	This instruction signals the end of the instruction sequence. It is mandatory to this instruction in order to avoid leaving the system in a busy state permanently. No more instructions will be executed after the END instruction is called.
WAIT	0xA	The WAIT instruction forces the instruction pointer to remain in the current position for a number of clock cycles defined by Ncycles.
TRIGGER	0xB	The TRIGGER generates a hardware L1 trigger.

Table 2.7: Instruction Table

JUMP

Instruction Code	0 h

Jump or Loop Instruction

Instruction Coding

22 – 20	19 – 16	15	14 – 8	7 – 0
3	**0**	**JnL**	**N**	**ADDRESS**

Parameter	Description	Range
JnL	JUMP not LOOP	0 – 1
N	Number of Loops before continue	0 – 7F
ADDRESS	Address to which the instruction sequence pointer will jump	0 -- FF

Description

This instruction allows the instruction sequence pointer to jump into a user defined location in the instruction memory. There are two possible modes: JUMP mode and LOOP mode. In Jump mode, the bit JnL is set to “0”, the sequence pointer is directed to the location given by ADDRESS with no other conditions. In LOOP mode, the bit JnL is set to “1”, the sequence pointer will be directed to ADDRESS only if the current instruction has been called a number of times less or equal to N. When this number is reached, the sequence continues and does not jump.

Example

The following instruction sequence will loop 10 times on instruction 0x0005 and 0x0006, before continuing to instruction 0x0008.

Instruction Address	Instruction Code
0x0005	XXXXXX
0x0006	XXXXXX
0x0007	**0x308A05**
0x0008	XXXXXX

RS_STATUS

Instruction Code	1 h

Reset Status Register Instruction

Instruction Coding

22 20	19 16	15 0
3	**1**	**X**

Description

This instruction sends a reset to the ERRST register.

RS_TRCFG

Instruction Code	2 h

Reset Trigger Configuration Register

Instruction Coding

22 20	19 16	15 0
3	**2**	**X**

Description

This instruction sends a reset to the TRCFG register.

RS_TRCNT

Instruction Code	3 h

Reset Trigger Counter Instruction

Instruction Coding

22 20	19 16	15 0
3	**3**	**X**

Description

This instruction sends a reset to the TRCNT register.

CHRDO

Instruction Code	6 h

Send Channel Readout Instruction

Instruction Coding

22 … 20	19 … 16	15 … 0
3	**6**	**X**

Description

This instruction sends the ALTRO CHRDO command to all the channels whose front-end card is active (cf. Active Front-end card List) and whose corresponding bit in the Active Channel List (ACL) is set to “1”.

PMREAD

Instruction Code	7 h

Pedestal Read Instruction

Instruction Coding

22 20	19 16	15 13	12	11 0
3	**7**	**X**	**BLOCK**	**CHANNEL ADDRESS**

Parameter	Description	Range
BLOCK	Bit indicating a full pedestal memory transfer “0” or only a block “1”	0 - 1
CHANNEL ADDRESS	Channel Address to which the Pedestal Memory Write is sent	0 -- FFF

Description

This instruction sends the ALTRO PMADD (W) and PMDTA (R) commands to the channel with address CHANNEL ADDRESS and to all possible 1024 locations (BLOCK = 0) of the corresponding ALTRO pedestal memory or sends only a block that is defined in the register PMCFG (BLOCK = 1). The result is compared with the content of the Pattern memory of the RCU. Any error in the comparison sets the bit[0] of the ERRST status register to “1”.

PMWRITE

Instruction Code	8 h

Pedestal Write Instruction

Instruction Coding

22 20	19 16	15	14	13 12	11 0
3	**8**	**X**	**BLOCK**	**BCAST**	**CHANNEL ADDRESS**

Parameter	Description	Range
BCAST	The instructions is broadcasted to all channels	0 – 1
BLOCK	Bit indicating a full pedestal memory transfer “0” or only a block “1”	0 - 1
CHANNEL ADDRESS	Channel Address to which the Pedestal Memory Write is sent	0 -- FFF

Description

This instruction sends the ALTRO PMADD (W) and PMDTA (W) commands to the channel with address CHANNEL ADDRESS to all 1024 locations (BLOCK = 0) of the corresponding ALTRO pedestal memory or sends only a block that is defined in the register PMCFG (BLOCK = 1). The instruction is broadcasted to all channels if the bcast bit is set to “1”.

END

Instruction Code	9 h

End Instruction

Instruction Coding

22 20	19 16	15 0
3	**9**	**X**

Description

This instruction signals the end of the instruction sequence. It is mandatory to this instruction in order to avoid leaving the system in a busy state permanentely. No more instructions will be executed after the END instruction is called.

WAIT

Instruction Code	A h

Wait Instruction

Instruction Coding

22 – 20	19 – 16	15 – 0
3	**A**	**Ncycles**

Description

The WAIT instruction forces the instruction pointer to remain in the current position for a number of clock cycles defined by Ncycles.

TRIGGER

Instruction Code	B h

Trigger Instruction

Instruction Coding

22 – 20	19 – 16	15 – 0
3	**B**	**X**

Description

The TRIGGER instruction generates a hardware trigger (L1) that will be seen and treated as an external signal. The combination of this instruction with the WAIT and LOOP instructions can provide a programmable in-circuit arbitrary trigger generator.

Example

The following instruction sequence will generate 10 L1 triggers spaced by 128 times the RCU clock period, typically 25ns.

Instruction Address	Instruction Code
0x0000	0x3B0000
0x0001	0x3A00FF
0x0002	**0x308A00**
0x0003	0x390000

2.5 Trigger Running Modes

There are three trigger running modes available on the RCU:

- **Mode 0**: Default Mode. Only a software trigger can be generated, using the SWTRG instruction of the ALTRO instruction set.

Example of script sequence for software trigger:

```
r 0x2000
w 0x8000 0xffffffff
r 0x2001
r 0x2001
w 0x8000 –c AFL.dat        ---- Set active frontend card list
w 0x6400 –c ACL.dat        ---- Set active channel list
w 0x7000 0x64000a
w 0x7001 0x700064          ---- Set number of samples/channel to 100
w 0x7002 0x64000b
w 0x7003 0x700000          ---- Set ADC as data generator
w 0x7004 0x74001B          ---- SWTRG as ALTRO instruction
w 0x7005 0x3A0FFF          ---- WAIT a sufficient large amount of time
w 0x7006 0x740018          ---- L2 as ALTRO instruction
w 0x7007 0x360000          ---- CHRDO macro for all available channels
w 0x7008 0x740019          ---- Read Pointer increase
w 0x7009 0x308504          ---- Loop 5 times (generate 5 times L1-readout)
w 0x700A 0x390000
w 0x7801 0x000000          ---- Set trigger mode to default value
r 0x0
```

- **Mode 2**: L1-only. In this mode a single L1 signal is required. This can be a true external signal or a hardware trigger generated by the TRIGGER instruction of the RCU instruction set.

Example of script sequence for external L1 trigger:

```
r 0x2000
w 0x8000 0xffffffff
r 0x2001
r 0x2001
w 0x8000 –c AFL.dat
w 0x6400 –c ACL.dat
w 0x7000 0x64000a
w 0x7001 0x700064
w 0x7002 0x64000b
w 0x7003 0x700000
w 0x7004 0x390000
r 0x0
wait 1 s
w 0x7801 0x1001F4          ---- Set trigger mode to 2
```

Example of script sequence for hardware L1 trigger generated internally:

```
r 0x2000
w 0x8000 0xffffffff
r 0x2001
r 0x2001
w 0x8000 –c AFL.dat
w 0x6400 –c ACL.dat
w 0x7000 0x64000a
w 0x7001 0x700064
w 0x7002 0x64000b
w 0x7003 0x700000
r 0x0
wait 1 s
w 0x7801 0x1001F4
w 0x7000 0x3B0000          ---- Generate L1 internally
w 0x7001 0x3AFFFF          ---- WAIT
w 0x7002 0x308500          ---- Loop 5 times (generate 5 L1 triggers)
w 0x7003 0x390000
r 0x0                      ---- Execute sequence
```

- **Mode 3**: L1-L2. This mode requires both external L1 trigger and L2_accept or L2_reject to be asserted.

Example of script sequence for external L1-L2 sequence trigger:

```
r 0x2000
w 0x8000 0xffffffff
r 0x2001
r 0x2001
w 0x8000 –c AFL.dat
w 0x6400 –c ACL.dat
w 0x7000 0x64000a
w 0x7001 0x700064
w 0x7002 0x64000b
w 0x7003 0x700000
r 0x0
wait 1 s
w 0x7801 0x1801F4          ---- Set trigger mode to 3
```

2.6 Debugging Sequence

The following instruction sequence is thought for electrical debugging.

Infinite Write / Read Instruction

- **Executing 0x0000** will configure produce an infinite number of ALTRO write instructions to given register and to a given channel. This sequence can be useful for probing the *cstb*, *ackn* or other ALTRO control signals.
- **Executing 0x0003** will configure produce an infinite number of ALTRO read instructions to given register and to a given channel.

Address	Value
0x7000	690000
0x7001	79000F
0x7002	300000
0x7003	590000
0x7004	300003

Chapter 3

Monitoring and Safety Module

3.1 Functionality

The Monitoring and Safety Module controls the power state, voltages, currents and temperature of the FECs. In detail, every FEC contains a 10-bit, 5-channel ADC with an on-chip temperature sensor and an I2C® interface. One channel is reserved to read the temperature, while the other 4 are fed with 2 voltages and 2 currents (analogue and digital) measured at the input of the FEC. The BC logic includes an I2C® master to read this ADC. The communication between the two units is synchronized by a clock signal with a frequency of 150 KHz. At this rate, every 2ms the BC reads the 5 parameters and updates the corresponding registers. In addition, the BC contains the configuration, status and error registers, and a set of counters that measure a number of critical signals (e.g. the Level-1 and Level-2). The table is accessible both via the ALTRO bus (during the configuration phase) and the Front-end Control Bus (in the configuration phase and data taking phase).

At power-up, the RCU downloads into the BC the reference range for the monitored quantities. As soon as one of these parameters goes out of range, the BC asserts the interrupt. The RCU starts polling the error register of each FEC to identify the error source. In the event of an hard error (temperature or currents over thresholds, voltage under thresholds, card power regulators error), the RCU switches off immediately the corresponding FEC. Immediately after a recovery procedure will be executed to diagnose the occurred error and report to the DCS system. It is important to note that, during these operations, the communication to the other cards of the branch is not perturbed.

3.2 Register Table

Name	Size	Base Address	Description
RESULT	21bit	0x8002	BC register from the SC read transactions
ERROR	2bit	0x8003	Error Register
INTmode	2bit	0x8004	Enable Interrupt
SCadd	16bit	0x8005	Address field for the SC commands
SCdata	16bit	0x8006	Data field for the SC commands
StatusMemory	16bit x 32	0x8100	Status Register (with Interrupt)

Table 3.1: Addressable Registers and Memory in the Monitoring and Safety Module

Name	Base Address	Description
SCcmd	0x8010	Execute Slow Control Command (option 2)
rst_ERRORreg	0x8011	Reset the Error Register
rst_RESULTreg	0x8012	Reset RESULT register
SCcmd	0xCxxx	Slow Control Command (option 1)

Table 3.2: Command in the MSM

3.3 Commands from the DCS

The Monitoring and Safety Module controls the state of the FECs. If the Interrupt is not active, the Monitoring and Safety Module receives **commands** from the Detector Control System (DCS) to monitor different parameter of the FECs. In this section the format of the SC commands is described.

The SC commands can be sent using two different formats. (1) One single command. (2) Two 16-bit registers (SCadd and SCdata) plus one command. While the option (1) allows the DCS to address up to 32 BC registers, the option (2) has an address field of 8 bits (up to 256 registers in the Board Controller).

The command format defined by the option (1) is the follwing:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				RnW	bcast	branch	FEC address					BC register address			

In the case of the option (2), the SCadd register is used to define the BC register address and the transaction mode (write or read cycle). The SCdata is used during write cycles with the data to be written.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	RnW	bcast	branch	FEC address				BC register address							

Table 3.3: Definition of the SCadd register for the Monitoring and Safety Module

In both cases, the SC transaction requires 8 µs. In read mode, the BC register is written in the RESULT register (0x8002).

Next section lists the BC register address field. For the TPC electronics, the BC register are encoded in 5 bits which are shown in the next table.

BC register address for the ALICE TPC Board Controller

These registers correspond to the Register Table in the Board Controller of each FEC. The address and meaning of each parameter is described in the next table. After the table, the Configuration Status Registers (CSR0, CSR1, CSR2 and CSR3) are explained.

Register Add	Mnemonic	Register Name	Width	Access Mode	Allow Bcast	Default Value
01	T_TH	Temperature Threshold	10	R/W	Y	**40 ºC**
02	AV_TH	Analog Voltage Threshold	10	R/W	Y	**3.61 V**
03	AC_TH	Analog Current Threshold	10	R/W	Y	**0.75 A**
04	DV_TH	Digital Voltage Threshold	10	R/W	Y	**2.83 V**
05	DC_TH	Digital Current Threshold	10	R/W	Y	**1.92 A**
06	TEMP	Temperature	10	R	N/A	**40 ºC**
07	AV	Analog Voltage	10	R	N/A	**3.61 V**
08	AC	Analog Current	10	R	N/A	**0.75 A**
09	DV	Digital Voltage	10	R	N/A	**2.83 V**
0A	DC	Digital Current	10	R	N/A	**1.92 A**
0B	L1CNT	L1 Counter	16	R	N/A	**0**
0C	L2CNT	L2 Counter	16	R	N/A	**0**
0D	SCLKCNT	Sampling Clock Counter	16	R	N/A	**0**
0E	DSTBCNT	Data Strobe Counter	8	R	N/A	**0**
0F	TSMWORD	Test Mode Words	9	R/W	Y	**1**
10	USRATIO	Under Sampling Ratio	16	R/W	Y	**1**
11	CSR0	Configuration Status Register 0	11	R/W	Y	**3FF**
12	CSR1	Configuration Status Register 1	14	R/W	Y	**0**
13	CSR2	Configuration Status Register 2	16	R/W	Y	**F**
14	CSR3	Configuration Status Register 3	16	R/W	Y	**2220**
Commands						
16	CNTLAT	Counters Latch	-	W	Y	-
17	CNTCLR	Counters Clear	-	W	Y	
18	CSR1CLR	CSR1 Clear	-	W	Y	
19	ALRST	ALTRO Reset	-	W	Y	
1A	BCRST	BC Reset	-	W	Y	
1B	STCNV	Start Conversion mADC	-	W	Y	
1C	SCEVL	Scan Event Length	-	W	Y	
1D	EVLRDO	Read Event Length	-	W	N/A	
1E	STTSM	Start Test Mode	-	W	Y	
1F	ACQRDO	Read Acquisition Memory	-	W	N/A	

Table 3.4: Definition of the registers and commands in the Board Controller

Note:

The parameters measured by the monitor ADC in the FEC have the following factors of conversion:

PARAMETER	Register Address	Factor of conversion
Temperature	06	0.25 ºC / ADC count
Analog Voltage	07	4.3 mV / ADC count
Analog Current	08	17 mA / ADC count
Digital Voltage	09	4.3 mV / ADC count
Digital Current	0A	30 mA / ADC count

CSR0 BC

Error and Interrupt Mask

BC address	11
Width	11
Register Type	Configuration
Access Type	Read / Write
Default Value	3FF

Instruction Coding

10	9 8	7 … 0
cnv	**Error Mask**	**Interrupt Mask**

Description

Parameter	Description	Range (hex)
cnv	Conversion Mode: 0 monitor ADC starts conversion sending STCNV command 1 monitor ADC converts continuously	0 – 1
Error Mask	These two bits mask the assertion of the **Error line** if in the board there are some of the errors registered in CSR1 [9 : 8] 0 the error is masked 1 the error asserts the line	0 – 3
Interrupt Mask	These bits mask the bits of CSR1 [7:0] for the assertion of the **Interrupt line**	0 – FF

CSR1 BC

Error and Interrupt Flags

BC address	12
Width	14
Register Type	Status
Access Type	Read / Write

Instruction Coding

13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERRUPT	ERROR	SC instr error	ALTRO error	BC instr error	BC par_error	missed sclk	alps error	paps error	dc over th	dv under th	ac over th	av under th	temp over th

Description

Parameter	Description	Line asserted
temp over th	Temperature of the board is higher than the threshold T_TH	Interrupt Line
av under th	Analog voltage of the board is lower than the threshold AV_TH	Interrupt Line
ac over th	Analog current of the board is higher than the threshold AC_TH	Interrupt Line
dv under th	Digital voltage of the board is lower than the threshold DV_TH	Interrupt Line
dc over th	Digital current of the board is higher than the threshold DC_TH	Interrupt Line
paps error	PASA power supply error: the power regulator that supply the PASA asserts this error	Interrupt Line
alps error	ALTRO power supply error: the power regulator that supply the ALTRO asserts this error	Interrupt Line
missed sclk	Missing sampling clock: this flag is asserted if during the number of readout cycles specified by CSR3 [7 : 0] there is not any sampling clock cycle	Interrupt Line
BC par_error	This flag is the parity bit of the 20 most significant bits of the	Error Line

	ALTRO bus.	
BC instr error	This bit is asserted if the access to the BC Register Table from the ALTRO bus is wrong (ex: try to write a only read register)	Error Line
ALTRO error	The value of the ALTRO error is registered	-
SC instr error	This bit is asserted if the access to the BC Register Table from the Front-end Control Bus is wrong	-
ERROR	Value of the error line	-
INTERRUPT	Value of the interrupt line	-

CSR2 BC

BC address	13
Width	16
Register Type	Configuration
Access Type	Read / Write
Default Value	F

Instruction Coding

15 … 11	10	9	8	7	6	5	4	3	2	1	0
		ALTRO test mode						clock_en		paps_en	
HADD	Card isolated	Continuous TSM	ALTRO address			ADC address		adcclk_en	rdoclk_en	pasa_sw	altro_sw

Description

Parameter	Description	Access mode
HADD	Hardware address of the board	read
Card isolated		read / write
Continuous TSM		read / write
ALTRO address		read / write
ADC address		read / write
adcclk_en	It enables the distribution of the sampling clock	read / write
rdoclk_en	It enables the distribution of the readout clock	read / write
pasa_sw	This bit enables the power regulator that provides the voltage to the PASA	read / write
altro_sw	This bit enables the power regulator that provides the voltage to the ALTRO	read / write

CSR3 BC

BC address	14
Width	16
Register Type	Configuration
Access Type	Read / Write
Default Value	2220

Instruction Coding

15	14 … 8	7 … 0
cnv end	**ALTRO master - watch dog**	**rdclk / sclk warning ratio**

Description

Parameter	Description	Access mode
cnv end	In every transaction with the monitor ADC this bit is reset and set it to 1 when the readout of the mADC is finished	read
ALTRO master – watch dog		read/write
rdclk / sclk warning ration	Referred to the detection of the missing sampling clock	read/write

Examples of commands for the Monitoring and Safety Module (referred to the table 3.3):

- The next sequence writes 16'h30 in the T_TH register of the BC in FEC number 1, branch A

  option (1) w 0xC021 0x0030

  option (2) w 0x8005 0x0101

  w 0x8006 0x0030

  c 0x8010

- Read Analog Voltage (register address 5'h7) from the FEC number 3, branch B

  option (1) c 0xCA67

  option (2) w 0x8005 0x5307

  c 0x8010

- Send BC reset in broadcast

  option (1) c 0xC41A

  option (2) w 0x8005 0x201A

  c 0x8010

FEC AL

Front End Card Active List

Instruction Code	8000 h
Width	32
Register Type	Status
Access Type	Read / Write

Instruction Coding

	27											16		12												0
BRANCH B														BRANCH A												
	B	**A**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**		**C**	**B**	**A**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Description

The bits are set to “1” if the corresponding FEC is ON. The Monitoring and Safety Module changes the value to “0” if an Interrupt is sent from a specific FEC and the error responsible of that Interrupt can damage the card.

RDOL

Readout List

Instruction Code	8001 h
Width	32
Register Type	Status
Access Type	Read / Write

The Instruction Coding and the meaning of the bits are the same than in the FEC_AL. The Monitoring and Safety Module can remove one card from the Readout List if that card has a “soft” error; the card remains ON and is able to answer to the Front-end Control Bus.

StatusMemory

Instruction Code	8100 h
Width	16
Access Type	Read / Write

Instruction Coding

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt source not Identified	branch	FEC address				card ON / OFF	Hardware Interrupt	missing sclk	alps error	paps error	dc > th	dv< th	ac > th	av < th	temp > th
								BC CSR1 [7:0]							

Description

The StatusMemory is a memory with the information about the FECs responsible of an Interrupt. It shows which FEC asserted the interrupt, the reason and the status (ON or OFF). The first word is the number of 16bit words written in the memory. The rest of the words provide the status of every FEC involved in the Interrupt. The meaning of the bits is the following:

Interrupt not Identified: This bit is 1 if there was an Interrupt asserted by the error flag of the power regulators in the FEC (Hardware Interrupt). Is possible that the FEC responsible of the Interrupt still answer and its BC does not report any abnormal situation so, the RCU is not able to detect the problem. The Interrupt is not identified, only information about the branch can be detected (StatusMemory [4]). In the case of this bit is 0, the remaining bits give complete information of the Interrupt detected:

Card ON/OFF: There are two different groups of errors: the “hard” errors and the “soft” errors. When the interrupt is due to an error of the first group or the error described in the previous paragraph, the Monitoring and Safety Module switches off the card and the bit Card ON/OFF of the Status Register is 0. If the error belongs to the second group, the card remains ON. In all the cases the card is removed from the Readout List.

The soft errors are: over temperature, under voltages (analog and digital) and missing sampling clock. The hard errors are the over currents (analog and digital) and the power supplies errors related to the PASA and ALTRO voltage regulators.

Hardware Interrupt: This bit is asserted if there was an Interrupt but the FEC does not answer. Most probably the power regulator that supplies the BC FPGA and the transceiver had a problem. The card is switched off.

CSR1: These bits contain information about the origin of the Interrupt. They correspond with the bits CSR1 [7:0] of BC responsible of the Interrupt.

FEC address: Address of the FEC that generates that specific Interrupt.

RESULT

Instruction Code	8002 h
Width	21
Access Type	Read / Write

Instruction Coding

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEC Address					**BC register**															

Description

This register contains the result of a command sent by the DCS. The lowest 16 bits are the data stored in the specific register of the BC requested by the DCS.

Once the DCS sends the command, it must wait 8 µs before reading this register.

ErrREG

Error register

Instruction Code	8003 h
Width	2
Register Type	Status
Access Type	Read / Write

Instruction Coding

1	0
not acknowledge from the addressed FEC	Instruction to a not active FEC

Note: Both bits are updated in every transaction

INTmode

Interrupt Mode

Instruction Code	8004 h
Width	2
Register Type	Configuration
Access Type	Read / Write

Instruction Coding

1	0
Enable Interrupt BRANCH B	Enable Interrupt BRANCH A

Description

The bits of this register are 1 if the MSModule must handle the Interrupt once it is asserted by the FEC. The Interrupt can be disabled by the module if there was an “Interrupt Source not Identified”