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Trigger manual

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The triggers are processed by the TRUs and the TOR. The TRUs can be controlled by the DCS boards *alidcsdcb1584*, *1587*, *1586*, *1585*, *1595*, *1594*, *1593*, *1592*, *1588*, *1589*, *1590* and *1591*, whereas the TOR can be controlled by the DCS board *alidcsdcb*1572.

Before configuring, you need to go to alidcscom075, and then log on to these DCS boards. To log on to a DCS board, you just need to type the two last digits, e.g. "84" for *alidcsdcb1584*, except for the TOR, where one types "tor".

Before you configure the TRU, make sure that the low voltage and the FEE are on.

1. Check if the TRUs are on or off

For example: on *alidcsdcb1584*, type "**rcu-sh r 0x5100**" and you will get "**0x7fff7fff**" if both the TRUs and the FECs are on. The highest "**7fff**" represent the B branch, and the lowest "**7fff**" are for the A branch. The last bit of each "**7fff**" represents the TRU.

2. Initialize TRUs

Go to **/mnt/dcbrw/tru-dcs-share/tru_script**. Type "**./TRU_initial.sh**" to initialize the TRUs. This should be done on every DCS board on which the TRUs are going to be used.

After initialization, the screen looks like this:

A:0x8002:0x2033
0x8003:0
0x8002 0x4
0x8003:0
B:0x8002:0x102033
0x8003:0
0x8002 0x100004
0x8003:0

This step takes some time, so please wait until the terminal prompt comes back. After the initialization, the threshold is set to 0x100, and the pedestal and mask have been set.

3. Configure TOR

- Start Tinserver
  Type "**ps**" on *alidcsdcb1572* to check whether the **Tinserver** is running or not, if not, run "**./mnt/dcbrw/starttinserver**" and check again.

- Check firmware
  Go to **/mnt/dcbrw** and check if the firmware is there. Type "**rcu-sh r 0x27**", and you will get the version number. If you get "no target answer", the FPGA doesn't have firmware yet, you need program it by typing "**./program_tor tor_fpga4_080311.bin**". The version number is **0x53**.

- Initialize TOR
  Run "**rcu-sh b /mnt/dcbrw/set_register.scr**" to initialize the TOR. After the initialization, the default mode is normal mode.

4. *Set the mask on the TOR side*

Actually the mask is already set to **0xfffa, 0xff** by **set_register.scr**. Because 93_A, 93_B, and 95_A are not available now, so you need to write
"**rcu-sh w 0x1b 0xabfe**" to ignore them.

Then if the trigger rate is reasonable (reading register 0x1f), no more mask is need to set. Otherwise, you need to mask off the TRUs that have unreasonable triggers.

5. Check TRU trigger rate

Check the trigger rates for each TRU on *alidcsdcb1572*. Run
"**rcu-sh b read_counter_M2_in. scr**" to check module 2,
"**rcu-sh b read_counter_M3_in. scr**" to check module 3 and
"**rcu-sh b read_counter_M4_in. scr**" to check module 4.

Which value is concerned?
After you type "**rcu-sh b read_counter_M2_in. scr**", you will get this:
executing: r 0x38
0x38: 0
executing: wait 100 us
executing: r 0x39
0x39: 0
executing: wait 100 us
executing: r 0x3a
0x3a: 0

executing: wait 100 us
executing: r 0x3b
0x3b: 0
executing: wait 100 us
executing: r 0x3c
0x3c: 0x1
executing: wait 100 us
executing: r 0x3d
0x3d: 0x1
executing: wait 100 us
executing: r 0x3e
0x3e: 0
executing: wait 100 us
executing: r 0x3f
0x3f: 0
executing: wait 100 us

The value following "0x** :" is what you need to pay attention to. For instance, "0x3c: 0x1"
means the trigger rate for this TRU is 1 Hz.

If the LED system is off, all the values you get should be around 0x00 . If the value is very large, this TRU is not configured properly or the FEEs need to be reset. Try to reset the electronics in M2 and 3 by "**GoReady**" on the GUI for the FEE.
!! For M4 do "**Configure**" and then "**TriggerEnable**".
!! If you have done "**GoReady**" for M4, please reinitialize TRUs in M4.
And then try to read trigger rate again. You should mask off TRUs that have large values.

6. How to mask

After you type "**rcu-sh b read_counter_M2_in.scr**", you can get the number of triggers in 1 second for each TRU. The counter address, the corresponding TRUs and the bit you need to set to mask off (the corresponding bit is set to 0 to mask off) are described as follows:
Address TRUs the corresponding bit for mask (This is for module 2, the mask register is **0x1c** in TOR firmware)

0x38 84_B 0
0x39 87_B 1
0x3a 86_B 2

0x3b 87_B 3
0x3c 84_A 4
0x3d 87_A 5
0x3e 86_A 6
0x3f 85_A 7

Address TRUs the corresponding bit for mask (This is for module 3 and 4, the mask register is 0x1b.)

0x28 88_B 0
0x29 89_B 1
0x2a 90_B 2
0x2b 91_B 3
0x2c 88_A 4
0x2d 89_A 5
0x2e 90_A 6
0x2f 91_A 7

0x30 95_B 8
0x31 94_B 9
0x32 93_B 10
0x33 92_B 11
0x34 95_A 12
0x35 94_A 13
0x36 93_A 14
0x37 92_A 15

For example, if you get answer like this:
0x38 : 0x3ee
0x39 : 0x1
0x3a : 0x2
0x3b : 0x789
0x3c :0x2
0x3d :0x1
0x3e :0x3
0x3f :0x689
It means TRUs 84_B, 87_B, and 85_A are not working well, you need to mask them out by writing "**rcu-sh w 0x1c 0x76**" .

7. Check L0 counting rate

Check if the trigger to be sent to the CTP is reasonable or not. Type "**rcu-sh r 0x1f**", the value you get should be around **0x01**. If not, please check the

trigger rate for each TRU again as described in step 6.

8. Set busy time 800μs

Finally, 0x8340 should be written in the readout_ mask_register 0xaf by type "**rcu-sh w 0xaf 0x8340**".